



# **Time-Reversal Based Range Extension Technique for Ultra-wideband (UWB) Sensors and Applications in Tactical Communications and Networking**

Technical Report (Quarterly)

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Prepared by

Robert C. Qiu

**(Principal Investigator)**

together with

(Contributing Researchers at Wireless Networking Systems Lab)

Nan (Terry) Guo

Zhen (Edward) Hu

Peng (Peter) Zhang

Yu Song

Amanpreet Singh Saini

Corey Cooke

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Department of Electrical and Computer Engineering

Center for Manufacturing Research

Tennessee Technological University

Cookeville, TN 38501

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## Executive Summary

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal.

The over-the-air demonstration of the concept of time reversal for an ultra-wideband (UWB) radio has been achieved recently in our Lab. In particular, synchronization has been obtained over the air. This even is, indeed, a landmark in the development of UWB radios. Time reversal represents a new transceiver framework that is an alternative to the transceivers using OFDM and RAKE receiver.

The future work is to leverage this UWB radio test-bed. The methodology is to evolve the test-bed into an ultra-wideband cognitive radio. Toward the implementation of UWB cognitive radio, high-speed analog-to-digital (A/D) conversion is the bottleneck for the test-bed. For a baseband signal of 5 GHz, it may take decades before the conventional A/D—based on Shannon's sampling theorem—is sufficient. The revolutionary compressed sensing says that we can sample the signals using sub-Nyquist sampling rate. Can we handle 5 GHz or even larger bandwidth using compressed sensing?



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# Chapter 1

## Introduction

The over-the-air demonstration of the concept of time reversal for an ultra-wideband (UWB) radio has been achieved recently in our Lab. In particular, synchronization has been obtained over the air. This even is, indeed, a landmark in the development of UWB radios. Time reversal represents a new transceiver framework that is an alternative to the transceivers using OFDM and RAKE receiver. The future work is to leverage this UWB radio test-bed. The methodology is to evolve the test-bed into an ultra-wideband cognitive radio. There are several reasons to justify this long-term evolution:

- (1) In the future, it is hoped that all the radios are composed of FPGA/DSP/GPP; The dynamic spectrum access (DSC) is paramount for spectrum efficiency. For example, Wi-Fi and Wi-Max radios must co-exist with UWB radios for future Navy operations. A cognitive radio will provide a new paradigm.
- (2) The radio with wideband RF front-end and RF frequency agility is the most challenging issue for spectrum sensing. The radio under development is an ultra-wideband software-defined radio (SDR). A natural evolution is to add the spectrum sensing capability. Only the RF part will be revised. The rest of the system leaves unchanged. This approach will greatly reduce the risk of the evolution.
- (3) Our goal is to have a wideband cognitive radio test-bed of the largest bandwidth. The main purpose of this future test-bed is to explore advanced system algorithms for range extension.

Toward the implementation of UWB cognitive radio, high-speed analog-to-digital (A/D) conversion is the bottleneck for the test-bed. For a baseband signal of 5 GHz, it may take decades before the conventional A/D—based on Shannon's sampling theorem—is sufficient. The revolutionary compressed sensing says that we can sample the signals using sub-Nyquist sampling rate. Can we handle 5 GHz or even larger bandwidth using compressed sensing?





**Part I**

**Test-bed**

## Chapter 2

# Test-Bed Development Overview

In this document we will report our recent success in time reversal UWB test-bed development. On April 14, 2008, we demonstrated the very first time reversal UWB radio in our lab. The major parameters of the test-bed under test are as follows.

- bandwidth: 800 MHz
- center frequency: 4 GHz
- chip rate: 25 Mc/s
- bit rate: 6.25 Mb/s
- propagation channel: indoor NLOS, 5 m

Noticeable temporal focusing has been seen and successful data transmission has been experimentally demonstrated in this somewhat harsh environment. Encouraged by this historical demonstration, we will continue the project toward next goals—system improvement and double transmission distance (see milestones list in Table 2.1). To achieve these in one year, there will be a body of challenging jobs including transplanting the receiver back-end from the Virtex-2 platform to the Virtex-5 platform, increase of the prefilter length, and solving the dynamic range problem, etc.

Table 2.1: Milestones

X	Stable Architecture	Q3 2007
X	Arbitrary Waveform Generating	Q1 2008
X	Time Reversal System (baseline)	Q2 2008
	Full-Function Time Reversal (double distance)	Q1 2009
	Performance Test and Trials	Q3 2009
	Potential Technology Transfer to US Navy	Q4 2009

## Chapter 3

# Implementation Work Conducted in the Last Quarter

### 3.1 Introduction

At the testbed's transmitter side, there are mainly five parts: Xilinx Virtex-5 LXT Prototype Platform, Fujitsu DK86064 DAC Evaluation Kit, TRF3703-15 Quadrature Modulator Evaluation Module, PSA4000A Local Oscillator Evaluation Board and Mini-Circuits ZVE-8G Amplifier, as shown in Figure 3.1.

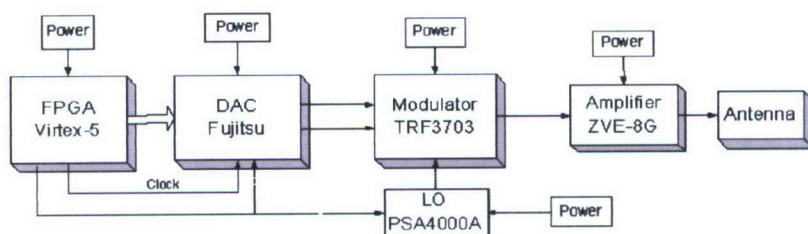


Figure 3.1: The architecture of transmitter side.

From functionality point of view, the testbed can be divided into two parts. One is the baseband arbitrary waveform generator which is made up of Xilinx Virtex-5 LXT Prototype Platform and Fujitsu DK86064 DAC Evaluation Kit. The other is the RF front-end which includes TRF3703-15 Quadrature Modulator Evaluation Module, PSA4000A Local Oscillator Evaluation Board and Mini-Circuits ZVE-8G Amplifier. However, the high-speed connection between Xilinx Virtex-5 LXT Prototype Platform and Fujitsu DK86064 DAC Evaluation Kit is the bottleneck for the system implementation, so we will especially address this important issue.



### 3.2 Baseband Arbitrary Waveform Generator

At the transmitter side, Xilinx Virtex-5 LXT Prototype Platform and Fujitsu DK86064 DAC Evaluation Kit are employed to build the baseband arbitrary waveform generator. This arbitrary waveform generator can generate the continuous baseband waveform for general purpose of communication or remote sensing. The picture of the baseband arbitrary waveform generator is shown in Figure 3.2. The diagram of the baseband arbitrary waveform generator is shown in Figure 3.3.

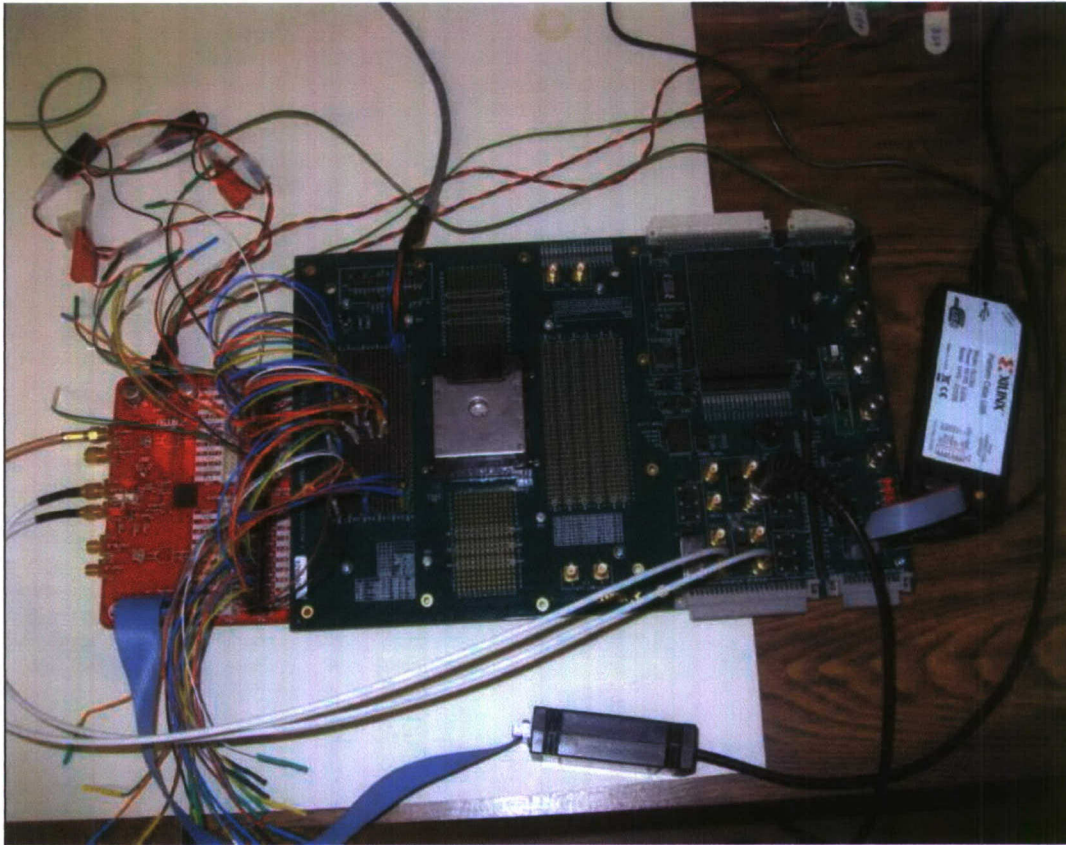


Figure 3.2: The picture of the baseband arbitrary waveform generator in the transmitter side.

From functionality point of view, the functionalities in Virtex-5 FPGA can be divided into two modules. One is the baseline transmitter module and the other is the waveform generator module. The baseline transmitter module generates sequences of '1' or '0' at the chip rate of 25 Mcps and the corresponding scrambling code. Figure 3.4 shows how to generate the scrambling code. The initial values for all shift registers are 1s. Discrete-time waveform is generated by the waveform generator module in FPGA based on chip value, scrambling code and the pre-loaded waveform template. Figure 3.5 shows the implementation of the waveform generator module. The discrete-time waveform is then fed to the DAC via the high-speed connection buses. Because of the limitation of the high-speed connection, only 2 bits are used to represent the continuous waveform in the digital domain. Owing to the introduction of scrambling code, the ternary quantization of the continuous waveform is implemented in FPGA. If the waveform is 4 ns pulse, the functionalities in FPGA is shown in Figure 3.6. Figure 3.7 shows the results observed from ChipScope. If the waveform is time reversed channel impulse response, the functionalities in FPGA is shown

in Figure 3.8. Figure 3.9 shows the results observed from ChipScope.

In the testbed, Fujitsu DK86064 DAC Evaluation Kit is connected to Xilinx Vitex-5 LXT Prototype Platform and MB86064 chip in Fujitsu DK86064 DAC Evaluation Kit converts the digital domain waveform to the analog domain waveform in the baseband. If the waveform is 4 ns pulse, then the input RF clock is 125 MHz and the sampling rate is 250 MHz; single DAC, LVDS data port A and driving DAC A pattern is used. In this situation, the functional block diagram of DAC is shown in Figure 3.10; the content of the WMM register settings file reg\_wmm.txt is shown in Table 3.2. Figure 3.11 shows the output of DAC if 4 ns pulse is generated. By routing external LVDS data through the waveform memory module, it is possible to interleave port A and port B data into one of the DAC cores. In this way, sampling rate can be doubled from that of each port to that of DAC core. Figure 3.12 shows interleaved mode odd and even data sampling. So if the waveform is time reversed channel impulse response, then input RF clock is 250 MHz and the sampling rate is 500 MHz; multiplexed LVDS data into DAC A pattern is used. In this situation, the functional block diagram of DAC is shown in Figure 3.13; the content of the WMM register settings file reg\_wmm.txt is shown in Table 3.2. Figure 3.14 shows the output of DAC if time reversed channel impulse response is generated.

Table 3.1: The content of the WMM register settings file if 4 ns pulse is generated.

Register address	Register value
0x0	0x0
0x10	0x2
0x11	0x0
0x20	0x2
0x21	0x0
0x12	0x0
0x22	0x0



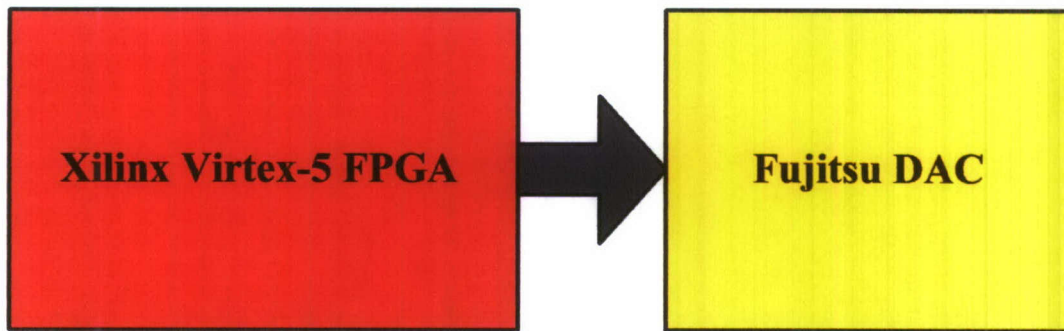


Figure 3.3: The diagram of the baseband arbitrary waveform generator in the transmitter side.

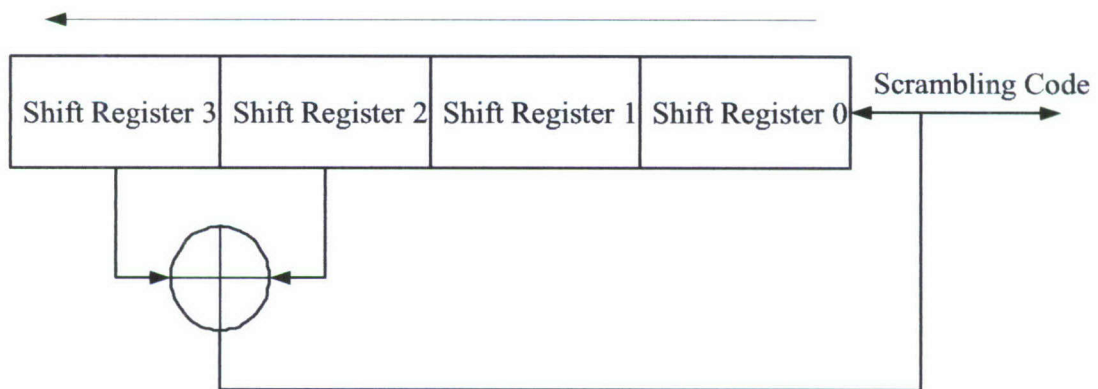


Figure 3.4: How to generate the scrambling code.

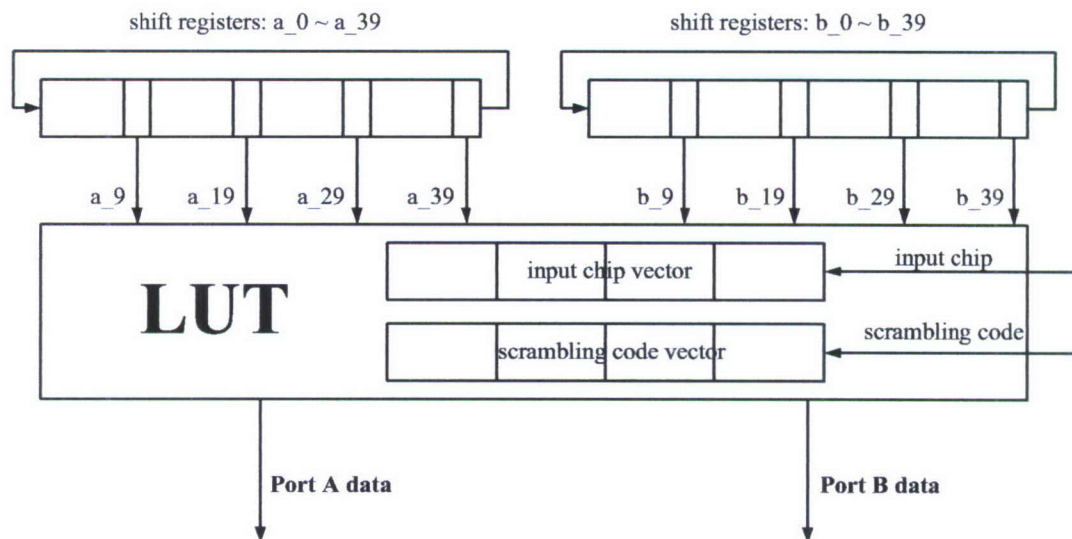


Figure 3.5: The implementation of the waveform generator module.

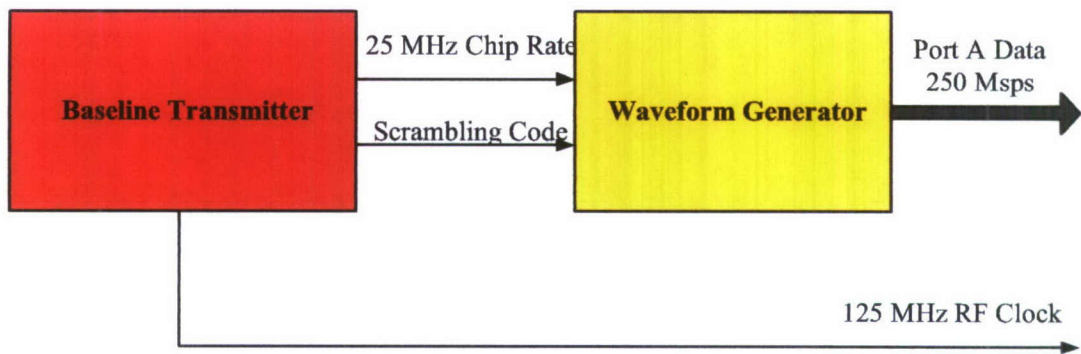


Figure 3.6: The functionalities in Virtex-5 FPGA if 4 ns pulse is generated.

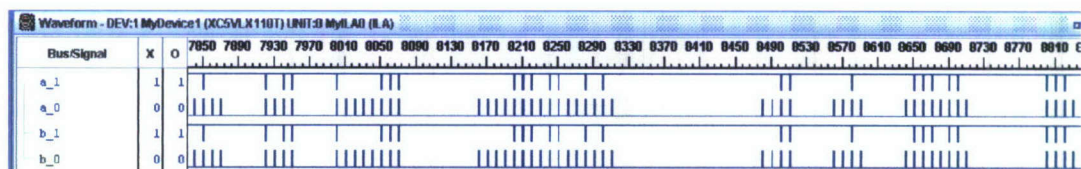


Figure 3.7: The results observed from ChipScope if 4 ns pulse is generated.

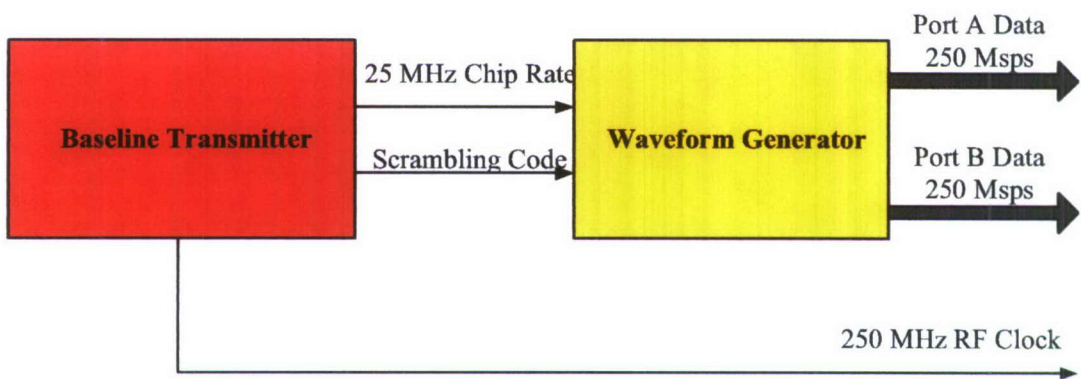


Figure 3.8: The functionalities in Virtex-5 FPGA if time reversed channel impulse response is generated.

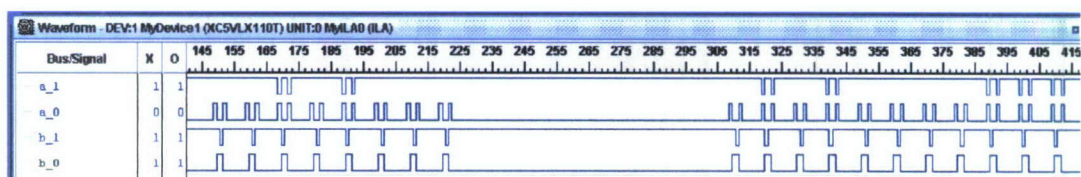


Figure 3.9: The results observed from ChipScope if time reversed channel impulse response is generated.



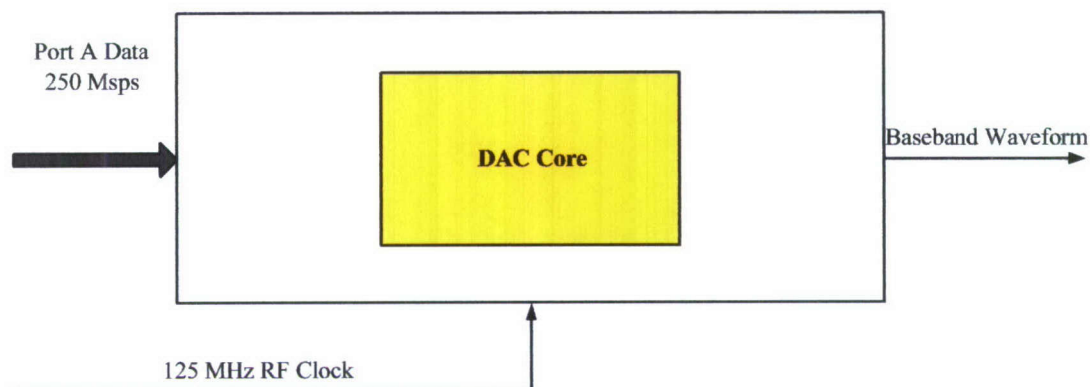


Figure 3.10: The functional block diagram of DAC if 4 ns pulse is generated.

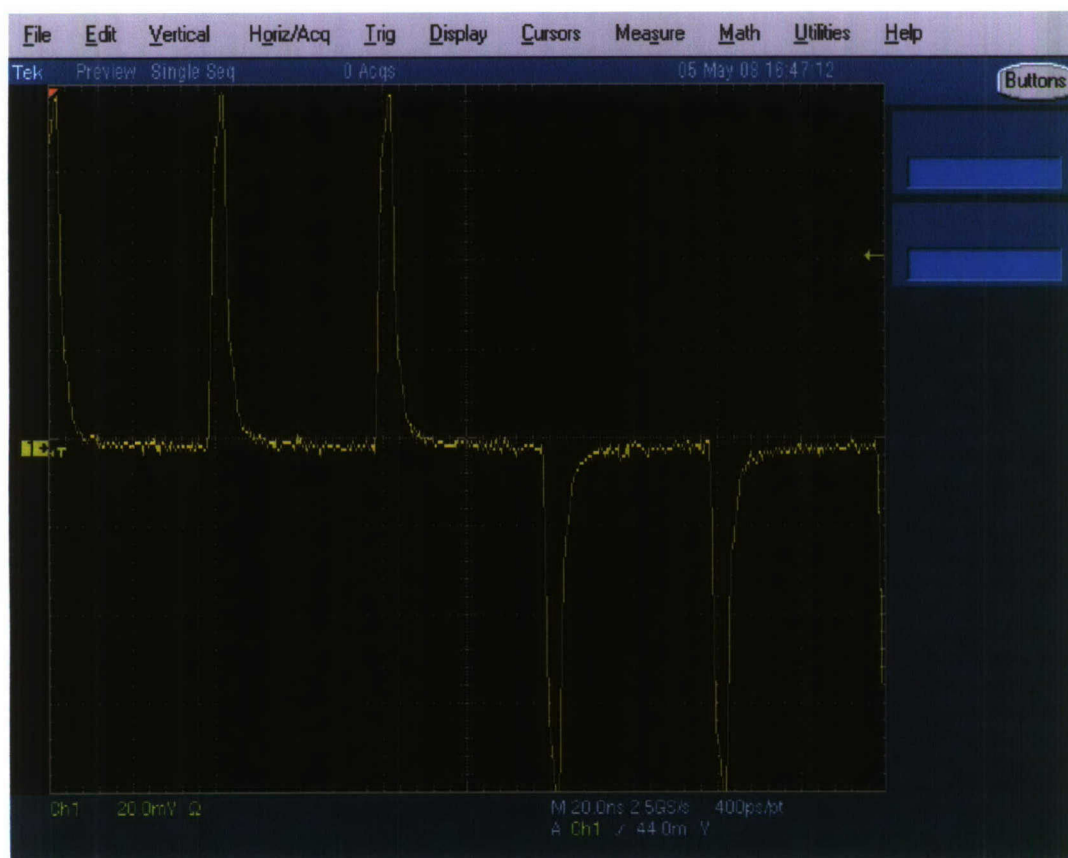


Figure 3.11: The output of DAC if 4 ns pulse is generated.

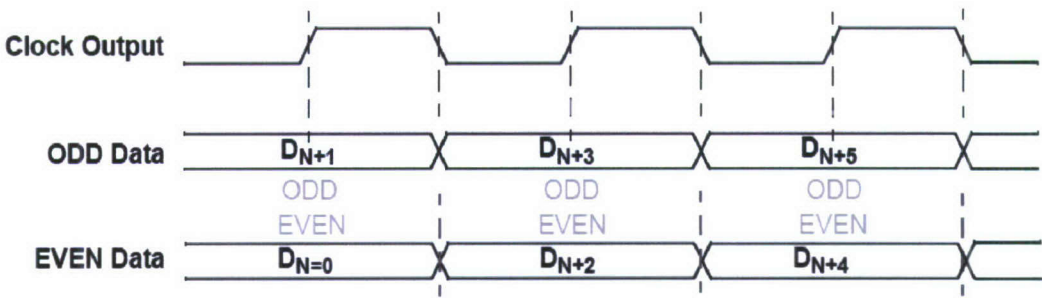


Figure 3.12: Interleaved Mode ODD and EVEN Data Sampling.

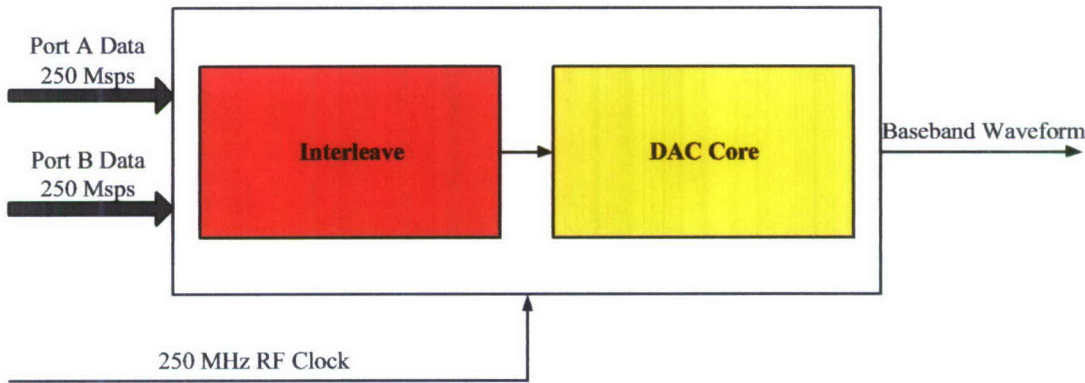


Figure 3.13: The functional block diagram of DAC if time reversed channel impulse response is generated.

Table 3.2: The content of the WMM register settings file if time reversed channel impulse response is generated.

Register address	Register value
0x0	0x10
0x10	0x2
0x11	0x10
0x20	0x2
0x21	0x1
0x12	0x0
0x22	0x0



Figure 3.14: The output of DAC if time reversed channel impulse response is generated.

### 3.3 High Speed DAC/FPGA Interface

To load the waveform from FPGA to DAC, we need a custom wiring harness to interface the FPGA prototyping evaluation board (EVB) and the DAC development kit (DK). The EVB uses 0.1" pitch headers (Figure 3.15) for data input/output (IO). Flying leads are desired here since FPGA pin assignment is prone to change. On the DK, we can use ribbon cable to connect the 0.1" pitch header. The probe cable (Figure 3.16) provided by Intronix is perfect for interfacing these two devices. The ribbon socket side can be directly plugged into the DK and the flying leads can be wired to the EVB with flexibility. This cable supports high sampling rate up to 500 MHz. According to our measurement results, this cable can actually support sampling at 1 GHz. The two boards with interface are shown in Figure 3.17.



Figure 3.15: 0.1" pitch header is used on FPGA EVB.



Figure 3.16: Intronix probing cable is used to interface FPGA EVB and DAC DK.

#### 3.3.1 Limitation of the FPGA EVB

The FPGA supports up to 1.2 GHz LVDS output rate. However, this EVB is not designed for high speed applications. The output amplitude of most ports is too weak for DAC to detect when generating 250 MHz or above signals. So far, 22 pairs of LVDS ports with adequate amplitude level have been found, as shown in Table 3.3. For these ports, however, the output waveform is distorted. Figure 3.18 compares the output waveforms generated by 1 GHz, 500 MHz and 250 MHz data, and the pulse width is 1 ns, 2 ns and 4 ns, respectively. It can be observed that as the pulse width narrows, the amplitude decreases and the sidelobe becomes more significant. This is due to the non-linear effect of the EVB circuit. The sidelobe acts as intersymbol interference (ISI) and will affect the output of the DAC. According to the test results, 250 MHz data suffers no ISI. Due to this limitation, we can only use 250 MHz output rate. In order to achieve higher signal bandwidth, we feed two 250 MHz data channels into the DAC and then do the interleaving inside the DAC. The data rate after interleaving is 500 MHz.

#### 3.3.2 Limitation of the DAC DK

There is a problem in the DK. Since there are two DAC cores in the DK, it provides the capability to generate dual channel 14-bit resolution DAC output at 1 GHz sampling rate. However, the circuit of this DK does not support high resolution. When using all 14 bits, we found error at the DAC output. This error is related to the input pin pair A12



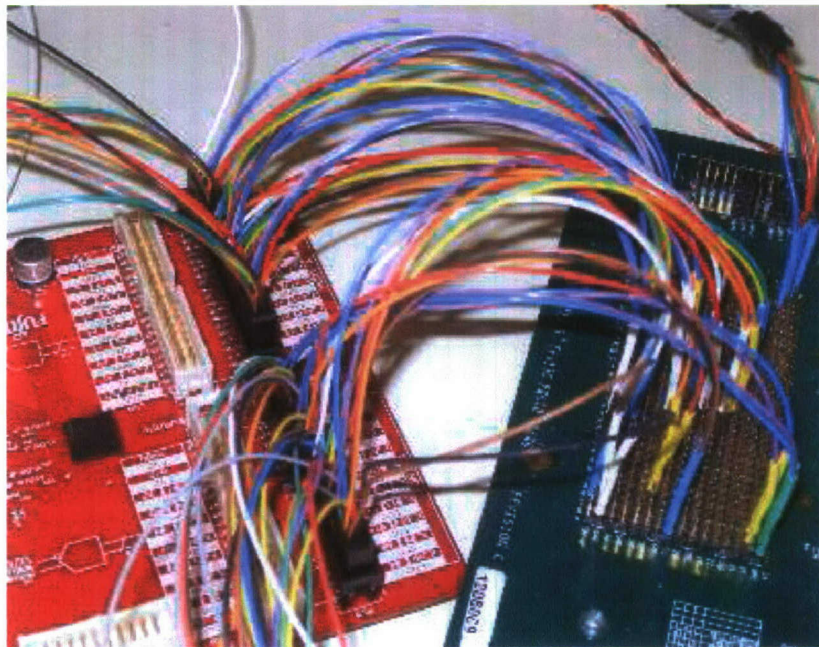


Figure 3.17: Connected FPGA EVB and DAC DK.

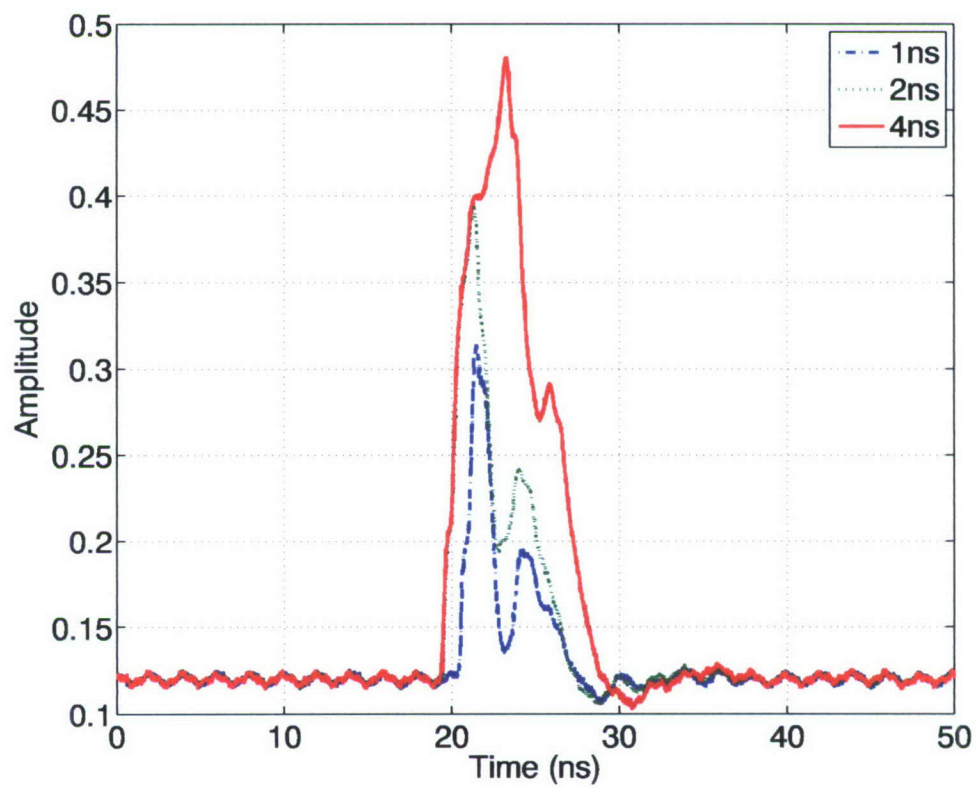


Figure 3.18: 1ns, 2 ns and 4 ns pulses measured at FPGA output pins.

Table 3.3: LVDS pin pairs for high data rate applications.

Pin #	Pin #
B30, A30	T30, U30
C25, B25	U28, U27
D34, C34	V27, V28
E31, F31	V29, W29
F34, G33	W25, V25
M33, N33	W26, Y26
N34, P34	W27, Y27
R27, R26	W30, V30
R31, T31	Y29, Y28
T26, U26	Y31, W31
T29, T28	AA31, AB31

and X\_A12. When turning this port off, no error is observed. This pin pair is the 3rd significant bit of DAC input. Hence, to avoid generating incorrect waveform, we use 2-bit resolution instead of 14-bit resolution.

According to the limitations mentioned above, the DAC requires the FPGA to provide two channels running at 2-bit resolution with 250 MHz sampling rate and one 250 MHz clock signal. The final pin assignment of the DAC and the FPGA is shown in Table 3.4.

Table 3.4: Pin assignment.

Port Name	FPGA Pin Description	FPGA Pin #	DAC Pin #
waveform_data_a.p <0>	IO_L15P_15	T28	A14
waveform_data_a.n <0>	IO_L15N_15	T29	X_A14
waveform_data_a.p <1>	IO_L6P_17	W31	A13
waveform_data_a.n <1>	IO_L6N_17	Y31	X_A13
waveform_data_b.p <0>	IO_L13P_15	T31	B14
waveform_data_b.n <0>	IO_L13N_15	R31	X_B14
waveform_data_b.p <1>	IO_L14P_11	P34	B13
waveform_data_b.n <1>	IO_L14N_11	N34	X_B13

### 3.4 Transmitter RF Front-End

We mainly rely on off-the-shelf products in our test-bed's RF development, major components and modules for transmitter side are listed in Table 3.5.

Table 3.5: A list of Selected Components/Modules for Transmitter

Local oscillator	PSA4000A	Z-communications	center frequency 4.0 GHz
Modulator (up-converter)	TRF3703-15	Texas Instruments	direct quadrature modulator 400 MHz to 4 GHz
Amplifier	ZVE-8G	Mini-circuits	wideband(2 to 8 GHz)/ low noise( 4 dB typ)

The test-bed's transmitter RF front-ends can be shown as Figure 3.19. Baseband signals from DAC are converted to passband signal by modulator and then be sent to the amplifier, the output signal of amplifier goes to the antenna and then be transmitted through the air.

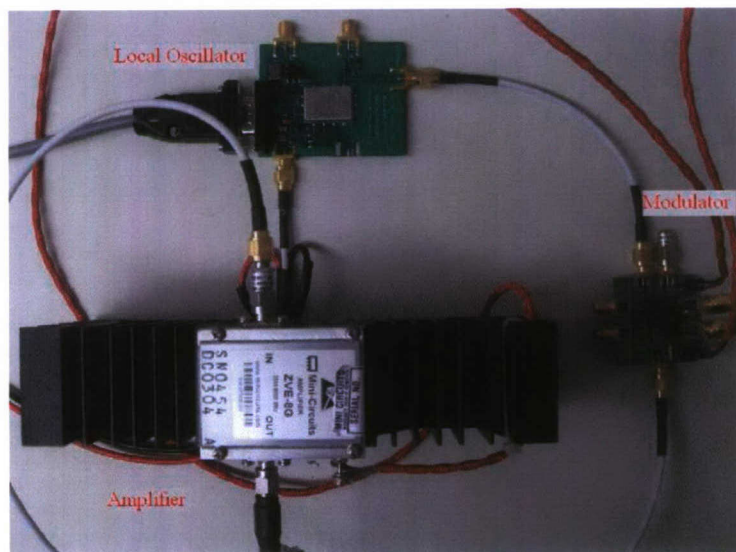


Figure 3.19: The picture of transmitter RF front-ends.

Local oscillator PSA4000A consists of a VCO with a PLL frequency synthesizer ADF4106 (made by Analog Devices). ADF4106 can be configured through an SPI port on the evaluation board. Here is an example of setting used in our test: power supply of +6 V, on-board 12MHz reference oscillator, phase frequency detector (PFD) reference frequency 1MHz, and VCO output frequency 4000MHz.

Quadrature modulator TRF3703-15 made by Texas Instruments is used as the up-converter. It is a very low-noise direct quadrature modulator, capable of converting complex modulated signals from baseband directly up to RF. The RF output block consists of a differential to single-end converter and an RF amplifier capable of driving a single-end 50Ω load without any need of external components.



ZVE-8G by Mini-circuits is a power amplifier operating from 2-8 GHz with +30 dB gain and a 1 dB compression point of 30 dBm. The unit requires a single 12 V 1.2 A supply.

### 3.4.1 Connection Between DAC and Modulator

Both the DAC's output and modulator's baseband input are differential type. RF transformer based AC coupling is used to bridge the DAC and modulator (see Fig.1). The advantage of using transformers is that they isolate the DC connection between the two devices but still provide wide bandwidth. The 82-ohm and 36-ohm resistors accommodate about 50 ohm input impedance and common mode voltage about 1.5 V required by the modulator.

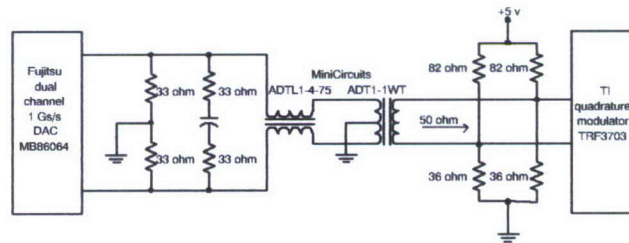


Figure 3.20: Coupling between DAC and modulator.

### 3.4.2 LO and DAC Configuration

In our system, there are several devices need to be configured before working, Such as local oscillator(LO) and Digital to analogy converter(DAC). We utilize SPI Bus protocol to implement this function with FPGA be the SPI master and other devices as SPI slaves. It shows that SPI Protocol is efficient and reduced system's complexity.

SPI standards for Serial Peripheral Interface, It is a simple interface that allows one chip to communicate with one or more other chips, it can easily achieve a few Mbps(mega-bits-per-seconds). Figure 3.21. shows A SPI master communicate with one slave and three slaves.

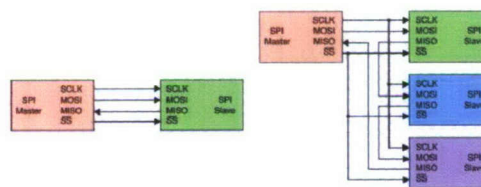


Figure 3.21: The block diagram of SPI Bus.

For Local oscillator, the Z-Communications' PSA4000A is supposed to be configured with the printer port of a PC computer as Figure 3.22 shows. We replace PC with the FPGA to write LO registers through the DB-9 interface.

PSA4000A mainly consists of two parts: ADF4106 and VCO. ADF4106 is a Frequency synthesizer from Analog Devices Co.Ltd., it works with one Voltage controlled oscillator (VCO) and one loop filter to implement a complete

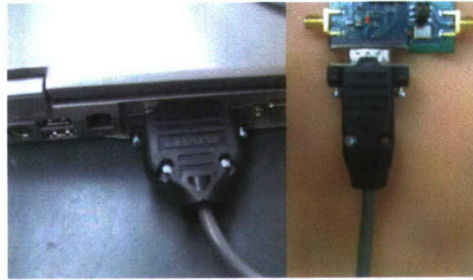


Figure 3.22: The picture of PC printer port used to configure local oscillator.

phase-locked loop(PLL), as shown in Figure 3.23, Where the ADF 4106 has a simple SPI compatible serial interface for writing to the device. CLK, DATA and LE control the data transfer, CE decides whether this device is chosen when there are more than one SPI slaves.

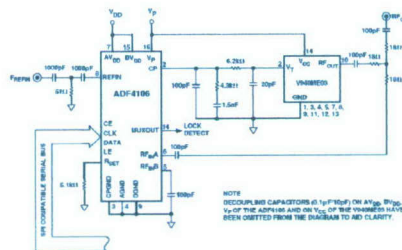


Figure 3.23: Block diagram of ADF4106 used to implement a local oscillator.

According to the datasheet of ADF4106, we generate the data with FPGA as shown in Figure 3.24. Which comes from the Logic analyzer. as a result, whenever FPGA is power on, the LO can be configured to work at 4.0GHz stably.

For DAC, its configuration and control are expected to through Fujitsu's PC USB programming cable and accompanying PC software as well as download test vectors to the waveform memory module, as shown in Figure 3.25, Where the DAC has 4 wire serial interface to implement configuration and control, as shown in Figure 3.26.

Similarly we use SPI protocol to control DAC, to facilitate this, an appropriate connector should be fitted to the target board providing connection to the signals as :SERIAL IN, SERIAL OUT, SERIAL CLK, and SERIAL EN.

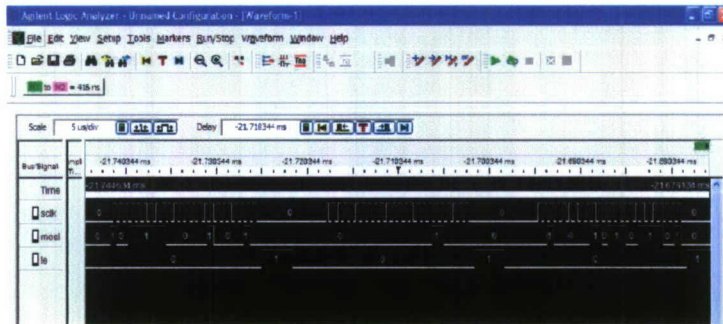


Figure 3.24: LO registers value generated by FPGA.

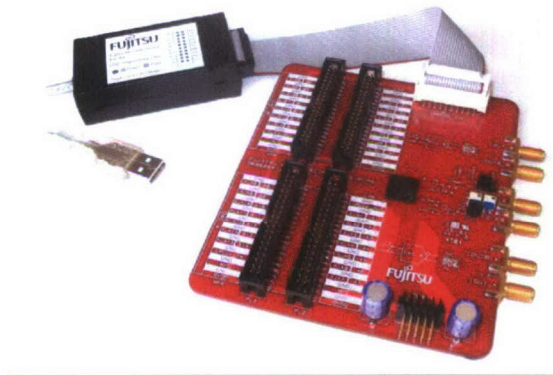


Figure 3.25: The diagram of DAC kit.

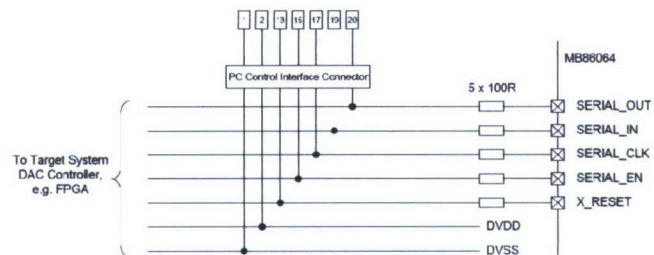


Figure 3.26: Recommended application PC control interface for DAC.



## Chapter 4

# Channel Sounding and Pre-filter with Practical Considerations

The central topic of this research is to take advantage of rich multipath propagation, which calls for a few key tasks: channel sounding and estimation as well as pre-filter optimization. There are many practical limitations in system implementation and here our concern on this matter is on the impact of passband sounding signal, and the practical pre-filter with limited sampling rate as well as small number of quantization bits. These non-ideal factors have to be taken into account in preparing the transmit waveforms. At center frequency 4 GHz, pre-filtering and estimating channel directly at RF are not realistic. For typical time-domain sounding, the sounding signal should be up-converted from baseband at the transmitter and down-converted back to baseband at the receiver. The received analog baseband sounding signal is then converted to digital domain for further processing. Since the signals are usually sparse, compressed sampling technique may be employed to sample the signal at sub-Nyquist rate. One important condition to achieve some sort of optimum is that the received baseband sounding waveform (called template)  $p(t)$  has to be known priorly. Generally this template differs from the transmit sounding waveform, because the transmitter-receiver RF chain acts as a filter and all circuit effect introduced over the radio link is taken into account by this template. In practice this template can be obtained via measurement. Because of the up- and down-conversion operation, the baseband signal has complex format. Accordingly, I/Q quadrature structure is used to generate and receive the complex signal. In the following discussion we will consider a channel with its channel impulse response (CIR)  $h(t)$  modeled as a tap delay line in a particular frequency range of interest:

$$h(t) = \sum_{k=1}^K \alpha_k \delta(t - \tau_k), \quad (4.1)$$

where  $\alpha_k$ 's are real numbers. This model does not take into account frequency-dependent distortion, but it is widely acceptable when the relative bandwidth is limited to a certain amount (say, 20%).

### 4.1 Time-Domain Channel Sounding and Channel Estimation

For convenient description in the following, complex representation is accepted to represent bandpass signals. Assume a bandpass sounding signal  $p(t)e^{j(\omega_c t + \theta_0)}$  is transmitted over the channel, where  $\omega_c$  is the carrier frequency



and  $\theta_0$  is an unknown initial phase. Up on receiving the noisy sounding signal

$$\begin{aligned} r(t) &= h(t) \otimes \left[ p(t) e^{j(\omega_c t + \theta_0)} \right] + n(t) \\ &= \sum_{k=1}^K \alpha_k p(t - \tau_k) e^{j[\omega_c(t - \tau_k) + \theta_0]} + n(t), \end{aligned} \quad (4.2)$$

the receiver's down-conversion stage outputs a baseband signal

$$\begin{aligned} y(t) &= \sum_{k=1}^K \alpha_k p(t - \tau_k) e^{j(-\omega_c \tau_k + \theta_0 + \theta_1)} + n'(t) \\ &= \left[ e^{j(\theta_0 + \theta_1)} \sum_{k=1}^K \alpha_k e^{-j\omega_c \tau_k} \delta(t - \tau_k) \right] \otimes p(t) + n'(t) \\ &= \left[ e^{j(-\omega_c t + \theta_0 + \theta_1)} \sum_{k=1}^K \alpha_k \delta(t - \tau_k) \right] \otimes p(t) + n'(t) \\ &= \left[ h(t) e^{j(-\omega_c t + \theta_0 + \theta_1)} \right] \otimes p(t) + n'(t) \\ &= \tilde{h}(t) \otimes p(t) + n'(t), \end{aligned} \quad (4.3)$$

where  $\theta_1$  is an unknown phase introduced in down-converting, “ $\otimes$ ” denotes convolution operation, and

$$\tilde{h}(t) = h(t) e^{j(-\omega_c t + \theta_0 + \theta_1)} = e^{j(\theta_0 + \theta_1)} \sum_{k=1}^K \alpha_k e^{-j\omega_c \tau_k} \delta(t - \tau_k) \quad (4.4)$$

is the frequency-shift version of the original CIR including an unknow rotation  $(\theta_0 + \theta_1)$ . Since the value of  $(\theta_0 + \theta_1)$  does not affect the system performance, in the following discussion it may be omitted. Frequency conversion also introduces a variable rotation  $-\omega_c t$ , resulting in a complex CIR.

There are a variety of estimation techniques to reduce the impact of noise  $n'(t)$  and multiple sounding pulses may be used in estimation. To describe the central idea conveniently, we assume perfect estimation here. The template  $p(t)$  can be measured by placing the transmit and receive antennas at a very short distance (say, 1 meter) to capture the direct path. Corresponding to the direct path, the received baseband sounding waveform can be expressed as

$$\left[ e^{j(\theta_0 + \theta_1)} \alpha_0 e^{-j\omega_c \tau_0} \delta(t - \tau_0) \right] \otimes p(t) + n'(t) = \alpha_0 e^{j(-\omega_c \tau_0 + \theta_0 + \theta_1)} p(t - \tau_0) + n'(t). \quad (4.5)$$

The estimate of  $p(t - \tau_0)$  can be obtained from the measured signal, where  $\tau_0$  is an unknown propagation delay. Without loss of generality,  $\tau_0 = 0$  can be assumed for simplicity.

Having known the template  $p(t)$ , based on the received sounding waveform  $y(t)$ , the frequency-shift CIR  $\tilde{h}(t)$  can be estimated using some matching based greedy algorithm such as CLEAN or matching pursuit algorithms.

## 4.2 Frequency-Domain Channel Sounding and Channel Estimation

Alternatively, if vector data (amplitude-angle pairs) can be measured, channel sounding and estimation can be done in frequency domain. A vector network analyzer (VNA) is able to measure/estimate the channel transfer function,

but implementing a frequency-domain channel sounding-estimation subsystem is not easy at all. Below we will only discuss its principle and will not touch how to design and implement the subsystem.

Let us ignore the background noise temporarily for simplicity. Denote by  $H(\omega)$  the channel transfer function and by  $W(\omega)$  a desired window function with support  $[\omega_1, \omega_N]$ , respectively.  $[\omega_1, \omega_N]$  has to cover the frequency of interest. Once the windowed transfer function

$$H_W(\omega) = W(\omega)H(\omega) \quad (4.6)$$

is obtained and the window function  $W(\omega)$  is known, we can find the frequency-shift CIR  $\tilde{h}(t)$ . Define  $p'(t)$ , the time-domain baseband representative for the inverse Fourier transform (IFT) of  $W(\omega)$ , by

$$IFT[W(\omega)] = w(t) = p'(t)e^{j\omega_c t}. \quad (4.7)$$

By left shifting the transfer function  $H_W(\omega)$  by  $\omega_c$ ,  $\omega_1 < \omega_c < \omega_N$ , and applying inverse Fourier transform, we have baseband waveform

$$\begin{aligned} IFT\{H_W(\omega + \omega_c)\} &= IFT\{W(\omega + \omega_c)H(\omega + \omega_c)\} \\ &= [w(t)e^{-j\omega_c t}] \otimes [h(t)e^{-j\omega_c t}] \\ &= p'(t) \otimes [h(t)e^{-j\omega_c t}] \\ &= p'(t) \otimes \tilde{h}(t). \end{aligned} \quad (4.8)$$

Realistically the baseband waveform is polluted by noise  $\eta(t)$  and thus can be expressed as

$$y'(t) = p'(t) \otimes \tilde{h}(t) + \eta(t). \quad (4.9)$$

Having known  $y'(t)$  and the artificial template  $p'(t)$ , the frequency-shift CIR  $\tilde{h}(t)$  can be estimated using any matching based deconvolution algorithms.

When using frequency-domain sounding, as the sounding sinusoidal sweeps from  $\omega_1$  to  $\omega_N$  at step  $\Delta\omega$ , a series of  $N$  frequency responses  $\{H_W(\omega_n)\}$  can be generated, where the background noise has been ignored. Based on  $\{H_W(\omega_n)\}$ , following the procedure described above, the frequency-shift CIR  $\tilde{h}(t)$  can be estimated. Of course, discrete-time inverse Fourier transform (DIFT), instead of continuous-time IFT, should be utilized.

### 4.3 Optimal Pre-Filter Coefficients Considering Implementation Limitations

Some optimization criterion has to be set in designing the pre-filter. It can be proved that by using  $\tilde{h}(T_0 - t)$  as a time reversal pre-filter, the received signal triggered by a single pulse would reach the maximum peak at time  $t = T_0$ . Time reversal is used in our test-bed as a simple optimal scheme. Now a problem rises: if implementing the pre-filter using a practical FIR filter (say, tap spacing 2 ns, 4-bit resolution, and 40 taps), what is the optimum set of the FIR filter coefficients?

Consider a length- $M$  FIR filter with tap spacing  $\Delta T$  and  $M$  quantized coefficients  $\{\beta_m\}$ , where  $\{\beta_m\}$  are normalized:

$$\sum_{m=1}^M \beta_m^2 = 1. \quad (4.10)$$



Assume the overall baseband waveform  $p(t)$  is known and satisfies

$$p(t) = 0, \text{ if } t < 0 \text{ or } t > \Delta T. \quad (4.11)$$

Note that the above assumptions lead to a constant transmit power corresponding to a single waveform  $p(t)$ . Let  $x(t)$  be  $p(t) \otimes \tilde{h}(t)$  and assume  $x(t)$  is defined in  $[t_a, t_b]$ . The FIR filter can be expressed as

$$f(t, t_0, \{\beta_m\}) = \sum_{m=1}^M \beta_m \delta(t - t_0 - m\Delta T), \quad (4.12)$$

where  $t_0$  is constant and  $M\Delta T \leq t_b - t_a$ . Being Triggered by a single pulse  $p(t)$ , the system outputs a baseband signal

$$\begin{aligned} f(t, t_0, \{\beta_m\}) \otimes p(t) \otimes \tilde{h}(t) &= \left[ \sum_{m=1}^M \beta_m \delta(t - t_0 - m\Delta T) \right] \otimes x(t) \\ &= \sum_{m=1}^M \beta_m x(t - t_0 - m\Delta T) \\ &= \sum_{m=1}^M \beta_m x(\Delta t - m\Delta T) \\ &\stackrel{\text{def}}{=} R(\Delta t, \{\beta_m\}), \end{aligned} \quad (4.13)$$

where  $\Delta t = t - t_0$ . The conditions “ $x(t)$  exists in  $[t_a, t_b]$ ” and “ $M\Delta T \leq t_b - t_a$ ” guarantee that  $R(\Delta t, \{\beta_m\})$  exists if  $\Delta t$  is in  $[t_a + M\Delta T, t_b + \Delta T]$ . Now we need to find the optimum coefficients  $\{\beta_m^{\text{opt}}\}$  that maximizes  $|R(\Delta t, \{\beta_m\})|$  at some time offset  $\Delta t = \Delta t_{\text{opt}}$ .

### 4.3.1 Case 1: ultra-fine quantization

In this case no quantization impact on the coefficients  $\{\beta_m\}$  should be taken into account. According to Cauchy-Schwarz inequality, the optimum coefficients for a given  $\Delta t$  are

$$\beta_m^{\text{opt}}(\Delta t) = \frac{x^*(\Delta t - m\Delta T)}{\sqrt{\sum_{i=1}^M |x(\Delta t - i\Delta T)|^2}}, m = 1, 2, 3, \dots, M; \quad (4.14)$$

where “\*” denotes conjugate operation and normalization has been applied. The corresponding output magnitude is

$$|R(\Delta t, \{\beta_m^{\text{opt}}(\Delta t)\})| = \sqrt{\sum_{m=1}^M |x(\Delta t - i\Delta T)|^2}. \quad (4.15)$$

Finally, the global optimum coefficients  $\{\beta_m^{\text{opt}}(\Delta t_{\text{opt}})\}$  are found by solving

$$\begin{aligned} \Delta t_{\text{opt}} &= \arg \max_{\Delta t} |R(\Delta t, \{\beta_m^{\text{opt}}(\Delta t)\})|^2 \\ &= \arg \max_{\Delta t} \sum_{m=1}^M |x(\Delta t - i\Delta T)|^2. \end{aligned} \quad (4.16)$$

It is not a great deal to find  $\Delta t_{\text{opt}}$  using numerical approach.

### 4.3.2 Case 2: real number restriction

Although the frequency-shift CIR is complex, the pre-filter can be reduced to having real-value coefficients only to simplify implementation further. Suppose a real set of optimum coefficients  $\{\beta_m^{opt}\}$  leads to a baseband output with maximum magnitude  $R_{max} > 0$  and reference angle  $\theta_{opt}$ ,  $0 \leq \theta_{opt} < \pi$ :

$$R_{max}e^{j\theta_{opt}} = \sum_{m=1}^M \beta_m^{opt} x(\Delta t_{opt} - m\Delta T) = \left| \sum_{m=1}^M \beta_m^{opt} x(\Delta t_{opt} - m\Delta T) \right| e^{j\theta_{opt}}, \quad (4.17)$$

or

$$R_{max} = \left| \sum_{m=1}^M \beta_m^{opt} x(\Delta t_{opt} - m\Delta T) \right| = \sum_{m=1}^M \beta_m^{opt} x(\Delta t_{opt} - m\Delta T) e^{-j\theta_{opt}}. \quad (4.18)$$

Note that the angular range is limited to  $\pi$  and the reason follows. If an angle  $\phi_{opt}$ ,  $\pi \leq \phi_{opt} < 2\pi$ , leads to a set of real coefficients  $\{\gamma_m^{opt}\}$ , then  $\{\beta_m^{opt}\} = \{-\gamma_m^{opt}\}$  would be the optimum set of real coefficients at  $\theta_{opt} = \phi_{opt} - \pi$ . Since only the real terms contribute to  $R_{max}$ , the above equation can be rewritten as

$$\begin{aligned} R_{max} &= \sum_{m=1}^M \beta_m^{opt}(\Delta t_{opt}, \theta_{opt}) \cdot \text{Re}[x(\Delta t_{opt} - m\Delta T) \cdot e^{-j\theta_{opt}}] \\ &= \sum_{m=1}^M \beta_m^{opt}(\Delta t_{opt}, \theta_{opt}) \cdot |x(\Delta t_{opt} - m\Delta T)| \cdot \cos(\angle^{x(\Delta t_{opt} - m\Delta T)} - \theta_{opt}), \end{aligned} \quad (4.19)$$

which implies that the optimum real coefficients  $\{\beta_m^{opt}(\Delta t_{opt}, \theta_{opt})\}$  are given by:

$$\beta_m^{opt}(\Delta t_{opt}, \theta_{opt}) = \frac{|x(\Delta t_{opt} - m\Delta T)| \cos(\angle^{x(\Delta t_{opt} - m\Delta T)} - \theta_{opt})}{\sqrt{\sum_{i=1}^M [|x(\Delta t_{opt} - i\Delta T)| \cos(\angle^{x(\Delta t_{opt} - i\Delta T)} - \theta_{opt})]^2}}, m = 1, 2, 3, \dots, M; \quad (4.20)$$

$$\begin{aligned} \{\Delta t_{opt}, \theta_{opt}\} &= \arg \max_{\Delta t, \theta} \left| \sum_{m=1}^M \beta_m^{opt}(\Delta t, \theta) x(\Delta t - m\Delta T) \right| \\ &= \arg \max_{\Delta t, \theta} \sqrt{\sum_{m=1}^M [|x(\Delta t - m\Delta T)| \cos(\angle^{x(\Delta t - m\Delta T)} - \theta)]^2} \\ &= \arg \max_{\Delta t, \theta} \sum_{m=1}^M [|x(\Delta t - m\Delta T)| \cos(\angle^{x(\Delta t - m\Delta T)} - \theta)]^2. \end{aligned} \quad (4.21)$$



### Mono-bit quantization

In this case we have  $\beta_m \in \{\pm 1/\sqrt{M}\}$ . Obviously, the above equations can be modified by taking polarization signs and normalizing using  $\sqrt{M}$ :

$$\beta_m^{opt}(\Delta t_{opt}, \theta_{opt}) = \frac{1}{\sqrt{M}} \text{sign}(\cos(\angle x(\Delta t_{opt} - m\Delta T) - \theta_{opt})), \quad m = 1, 2, 3, \dots, M; \quad (4.22)$$

$$\begin{aligned} & \{\Delta t_{opt}, \theta_{opt}\} \\ &= \arg \max_{\Delta t, \theta} \left| \sum_{m=1}^M \beta_m^{opt}(\Delta t, \theta) x(\Delta t - m\Delta T) \right| \\ &= \arg \max_{\Delta t, \theta} \sqrt{\sum_{m=1}^M \frac{1}{\sqrt{M}} \text{sign}(\cos(\angle x(\Delta t - m\Delta T) - \theta)) \cdot |x(\Delta t - m\Delta T)| \cos(\angle x(\Delta t - m\Delta T) - \theta)} \\ &= \arg \max_{\Delta t, \theta} \sqrt{\sum_{m=1}^M \frac{1}{\sqrt{M}} |x(\Delta t - m\Delta T)| \cos(\angle x(\Delta t - m\Delta T) - \theta)} \\ &= \arg \max_{\Delta t, \theta} \sum_{m=1}^M |x(\Delta t - m\Delta T)| \cos(\angle x(\Delta t - m\Delta T) - \theta). \end{aligned} \quad (4.23)$$

### Ternary quantization

Performance may be improved over mono-bit quantization when using ternary quantization, i.e.,  $\beta_m \in \{0, \pm u\}$ , with  $u$  being a positive number. Given a threshold  $v$ , the optimum real coefficients can be calculated in the following way:

$$\beta_m^{opt}(\Delta t_{opt}, \theta_{opt}) = \sum_{m=1}^M \frac{q_m(\Delta t_{opt}, \theta_{opt}, v)}{\sqrt{\sum_{i=1}^M q_i^2(\Delta t_{opt}, \theta_{opt}, v)}}, \quad m = 1, 2, 3, \dots, M; \quad (4.24)$$

$$\begin{aligned} & q_m(\Delta t, \theta, v) \\ &= \begin{cases} \text{sign}(\cos(\angle x(\Delta t - m\Delta T) - \theta)), & \text{if } |x(\Delta t - m\Delta T)| \cos(\angle x(\Delta t - m\Delta T) - \theta) \geq v, \\ 0, & \text{otherwise.} \end{cases} \end{aligned} \quad (4.25)$$

$$\begin{aligned} & \{\Delta t_{opt}, \theta_{opt}\} \\ &= \arg \max_{\Delta t, \theta} \sum_{m=1}^M \frac{q_m(\Delta t, \theta, v)}{\sqrt{\sum_{i=1}^M q_i^2(\Delta t, \theta, v)}} |x(\Delta t - m\Delta T)| \cos(\angle x(\Delta t - m\Delta T) - \theta) \\ &= \arg \max_{\Delta t, \theta} \frac{1}{\sqrt{\sum_{m=1}^M q_i^2(\Delta t, \theta, v)}} \sum_{m=1}^M |x(\Delta t - m\Delta T)| q_m(\Delta t, \theta, v) \cos(\angle x(\Delta t - m\Delta T) - \theta). \end{aligned} \quad (4.26)$$

Of course, there must be an optimum threshold  $v_{opt}$  for a given CIR  $\tilde{h}(t)$ , and theoretically it can be found using the similar technique applied above. The above optimization procedure for ternary quantization is not as easy as that for

mono-bit quantization, which motivates to find some suboptimal solutions. The optimization algorithm described below is such a solution.

#### ALGORITHM

$$\begin{aligned}
&\mathcal{M} = \{1, 2, 3, \dots, M\}; \\
&R_{max} = 0; \\
&\{\Delta t_{opt}, \theta_{opt}\} = \arg \max_{\Delta t, \theta} \sum_{m \in \mathcal{M}} |x(\Delta t - m\Delta T) \cos(\angle^{x(\Delta t - m\Delta T)} - \theta)|; \\
&R'_{max} = \frac{1}{\sqrt{M}} \sum_{m \in \mathcal{M}} |x(\Delta t_{opt} - m\Delta T) \cos(\angle^{x(\Delta t_{opt} - m\Delta T)} - \theta_{opt})|; \\
&N = M; \\
&\text{while } (N > 0) \& (R'_{max} > R_{max}); \\
&\quad N \leftarrow N - 1; \\
&\quad R_{max} \leftarrow R'_{max}; \\
&\quad u_m = \frac{1}{\sqrt{N}} \text{sign}(\cos(\angle^{x(\Delta t_{opt} - m\Delta T)} - \theta_{opt})), \quad m \in \mathcal{M}; \\
&\quad m' = \arg \min_m |x(\Delta t_{opt} - m\Delta T) \cos(\angle^{x(\Delta t_{opt} - m\Delta T)} - \theta_{opt})|; \\
&\quad \mathcal{M} \leftarrow \mathcal{M} - \{m'\}; \\
&\quad \{\Delta t_{opt}, \theta_{opt}\} = \arg \max_{\Delta t, \theta} \sum_{m \in \mathcal{M}} |x(\Delta t - m\Delta T) \cos(\angle^{x(\Delta t - m\Delta T)} - \theta)|; \\
&\quad R'_{max} = \frac{1}{\sqrt{N}} \sum_{m \in \mathcal{M}} |x(\Delta t_{opt} - m\Delta T) \cos(\angle^{x(\Delta t_{opt} - m\Delta T)} - \theta_{opt})|; \\
&\text{end (while)}
\end{aligned} \tag{4.27}$$

Here is the philosophy used in the algorithm: start with a case of all-non-zero coefficients (mono-bit case); if an increased baseband output is obtained, turn the least significant coefficients to zero, update the optimum pair  $\{\Delta t_{opt}, \theta_{opt}\}$  accordingly, and calculate new non-zero coefficient set  $\{u_m\}$ ,  $m \in \mathcal{M} \subseteq \{1, 2, 3, \dots, M\}$ ; repeat the procedure until no improvement is obtained. In this algorithm “turning the least significant coefficients to zero” does not guarantee to be a right decision, thus it is a suboptimal approach. The outcomes of this algorithm include  $N$  non-zero coefficients  $\{u_m\}$ ,  $m \in \mathcal{M} \subseteq \{1, 2, 3, \dots, M\}$ , and the suboptimal set of coefficients are given by

$$\beta_m = \begin{cases} u_m, & \text{if } m \in \mathcal{M}, \\ 0, & m = 1, 2, 3, \dots, M \text{ and } m \notin \mathcal{M}. \end{cases} \tag{4.28}$$

#### 4.3.3 Approximate approaches

Obtaining an optimum set of real coefficients needs multi-dimensional search. However, the optimization computation may be reduce by adopting some approximation techniques in deciding the reference angle.

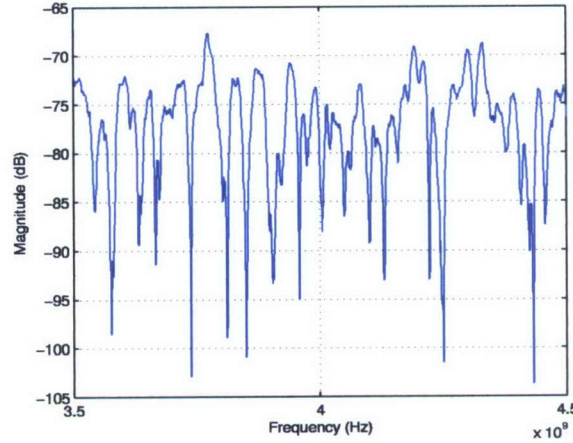


Figure 4.1: Rectangular windowed channel transfer function  $H_W(f)$  from VNA. Frequency starts from 3.5 GHz to 4.5 GHz, step = 1 MHz.

### Reduction of search space

For instance, a search space includes only four angles could be  $\{0, \pi/4, \pi/2, 3\pi/4\}$ . Actually, in most of rich multipath scenarios, the received baseband signal strength is not sensitive to  $\theta$ , implying that randomly selecting a reference angel  $\theta$  would not be too bad. On the other hand, for sparse multipath channel with a strong dominated path, if  $|x(\Delta t - m\Delta T)|$ ,  $m = 1, 2, 3, \dots, M$ , reaches maximum at  $m = m_1$  and  $\Delta t = \Delta t_1$ , then taking  $\angle x(\Delta t_1 - m_1\Delta T)$  as the reference angle  $\theta$  can be a suboptimal choice.

### Approximation of $\cos(\cdot)$

In addition, calculation of  $\cos(\angle x(\Delta t - m\Delta T) - \theta)$  may be approximated by

$$\cos(\angle x(\Delta t - m\Delta T) - \theta) = \begin{cases} 1, & \text{if } -\pi/4 \leq \angle x(\Delta t - m\Delta T) - \theta < \pi/4, \\ -1, & \text{if } 3\pi/4 \leq \angle x(\Delta t - m\Delta T) - \theta < 5\pi/4, \\ 0, & \text{otherwise.} \end{cases} \quad (4.29)$$

In our test-bed, we use this approximation to get a ternary quantized FIR filter. Figure 4.1 is a rectangular windowed transfer function  $H_W(f)$  captured by VNA, with 1 MHz frequency step. Figure 4.2 shows  $|x(t)| = |IFT\{H_W(f + f_c)\}|$ , with  $f_c = 4$  GHz. By setting  $\Delta T = 2$  ns,  $v = 25\% \max |x(t)|$ , we get FIR filter  $f(t, t_0, \{\beta_m\})$ , depicted in Figure 4.3.

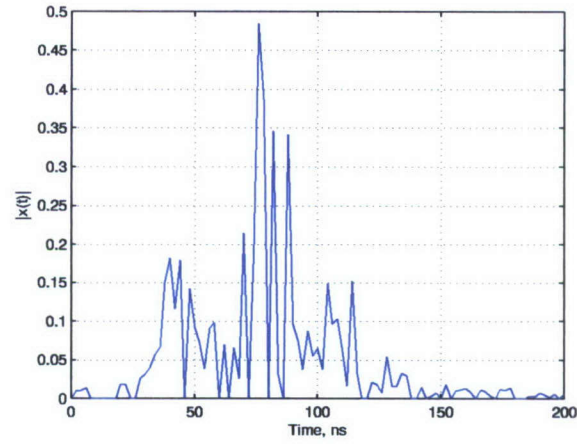


Figure 4.2:  $|x(t)| = |IFT\{H_W(f + f_c)\}|$  with  $f_c = 4$  GHz.

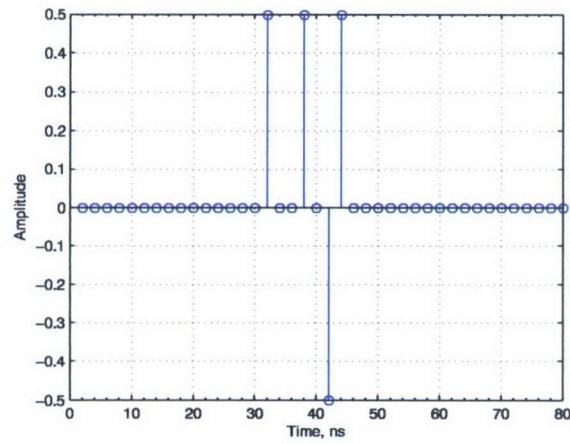


Figure 4.3: 40-tap ternary quantized FIR filter with  $\Delta T = 2$  ns,  $v = 25\% \max |x(t)|$ .





## Chapter 5

# System Test

In this chapter we will describe the system test of our time reversal test-bed. To the best of our knowledge, time reversal functionality and time focusing property was verified by test-bed for the first time.

### 5.1 System Test Setup

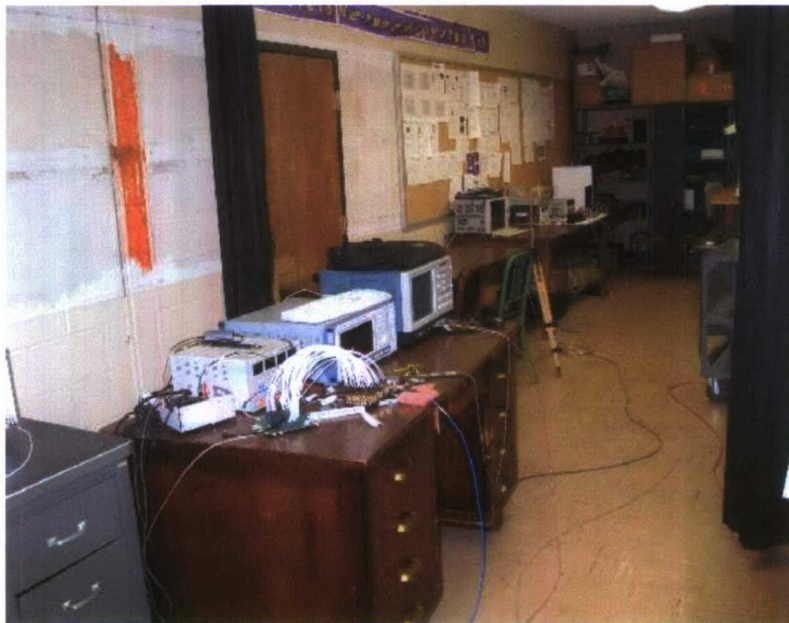


Figure 5.1: Room 400, compartment A.



Figure 5.2: Room 400, compartment B.

Our system test is performed in a typical non-line-of-sight (NLOS), three-compartment office environment. Transmitter and receiver are located in compartment A and compartment B, as can be seen from Figure 5.1 and Figure 5.2. There are wood and metal shelves, desks and chairs, computers and electronic equipments in both compartments. Figure 5.3 shows the layout of the office and the positions of the antennas. The transmit and receive antennas are NLOS. Multipaths can be obtained.

We first prepare the baseband time reversal waveform from the measurement mentioned in Chapter 3. During the measurement, no people is inside the office. Since the channel is tend to change after measurement, we try to maintain the positions of all the furnitures and equipments.

We transmit bit stream '1010110011110000' at 6.25 Mbps. Two kinds of waveforms are tested, time reversal waveform of our 2nd generation test-bed and single-pulse waveform of our 1st generation test-bed. For time reversal waveform, there are four 40-ns chips in each bit and several 2-ns pulses in each chip. The transmitted time reversal waveform captured by DPO is shown in Figure 5.4. Scrambling is applied with the method mentioned in Chapter 2. In this case, each chip is comprised of four pulses. Figure 5.5 is the spectrum of the modulated time reversal waveform captured by Spectrum Analyzer. The center frequency is 4 GHz and the 10 dB bandwidth is about 800 MHz.

For single-pulse waveform, the difference is that there is only one 4-ns pulse in each chip, as illustrated in Figure 5.6. Scrambling is applied. This is the setup of our 1st generation test-bed with scrambling. The spectrum of the modulated waveform is shown in Figure 5.7. The center frequency is 4 GHz and the 10 dB bandwidth is about 400 MHz.



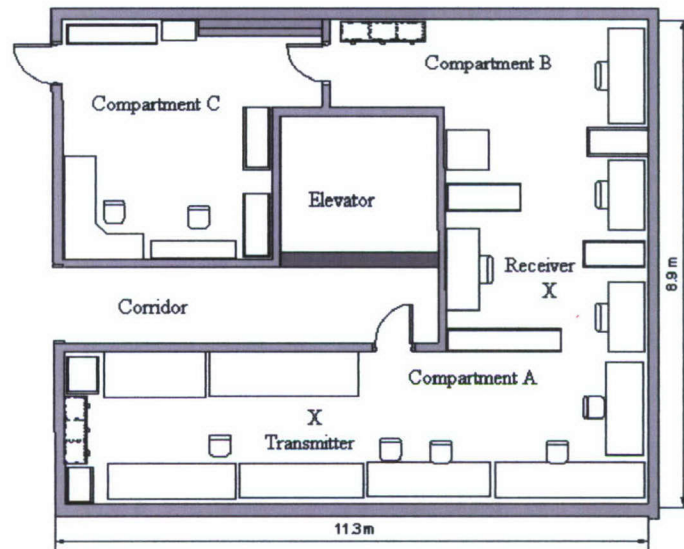


Figure 5.3: Room 400, layout.

The receiver structure is depicted in Figure 5.8. The detector output is a test point monitored by DPO. This is analog signal being sampled by ADC. Recovered bit stream is directly connected from an FPGA output port to DPO for observation.

## 5.2 Test Results

Figure 5.9 shows the system test result using time reversal waveform. The first trace is the transmitted waveform. The second trace is the detector output. The third trace is the bit stream. In the first trace, we can see that it is a zoom-out version of Figure 5.4. Distinguishable pulses can be observed in the second trace. In the third trace, we can clearly figure out the values of the bit stream. It is exactly the same as what is transmitted.

Figure 5.10 shows the system test result using the single-pulse waveform. We can see undistinguishable pulses due to the multipaths. The third trace is flat. It means that the bit stream from FPGA decision is always '1'. Hence we can say that the system is not working.

Here we give a close-up to the second trace of the time reversal waveform test result, shown in Figure 5.11. The first trace is the transmitted waveform. The second trace is the received waveform after detector. The third trace is the bit clock running at 6.25 MHz. Time focusing property can be observed by comparing the first trace and the second trace. At the transmitter side, each chip period has four pulses. While at the receiver side, after the channel, each chip period has only one pulse. Four pulses arrive at the same position in time axis after propagating through the channel. Pulses between chips are clearly separated. Some sidelobes can be observed, because we use 2-bit ternary quantization and there are only four pulses in each chip. However, from Figure 5.11, we can claim that, to the best



of our knowledge, the time focusing property of time reversal is verified by our test-bed for the first time.

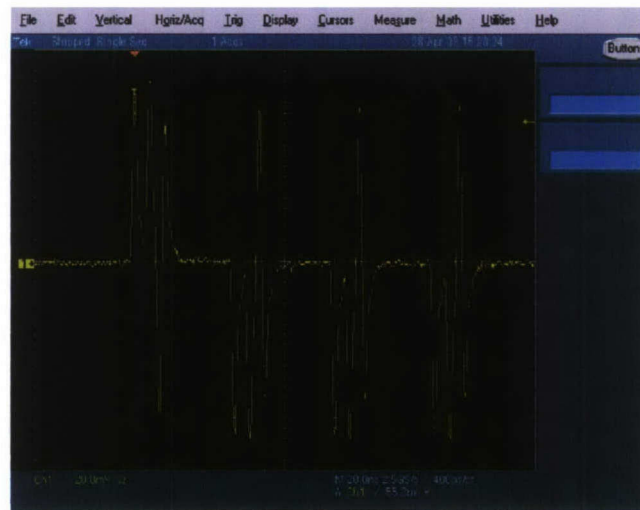


Figure 5.4: Baseband time reversal waveform with scrambling.

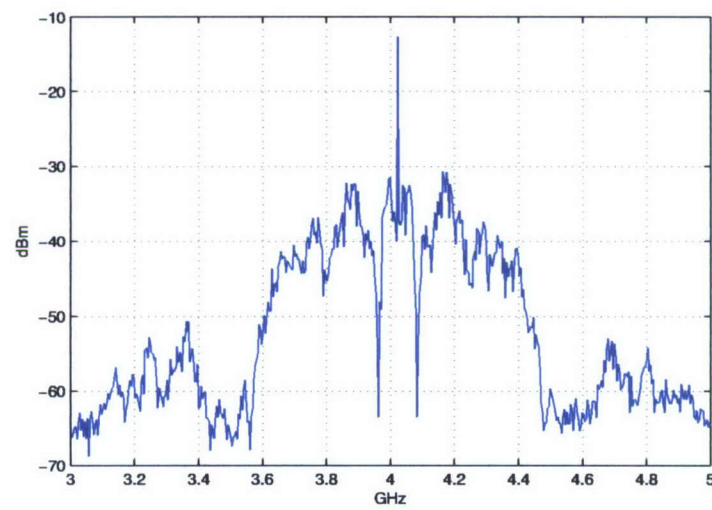


Figure 5.5: Spectrum of time reversal waveform after modulation.

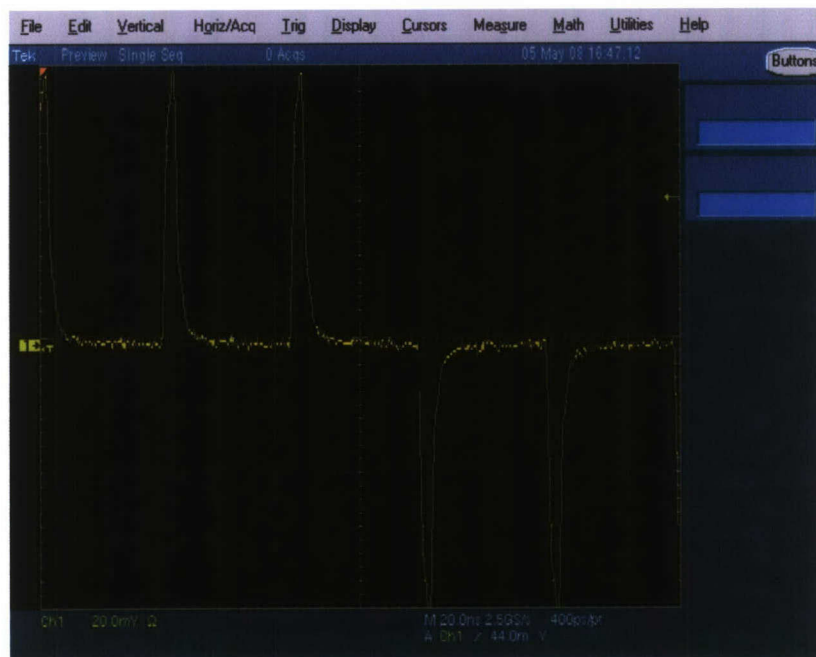


Figure 5.6: Baseband single-pulse waveform with scrambling.

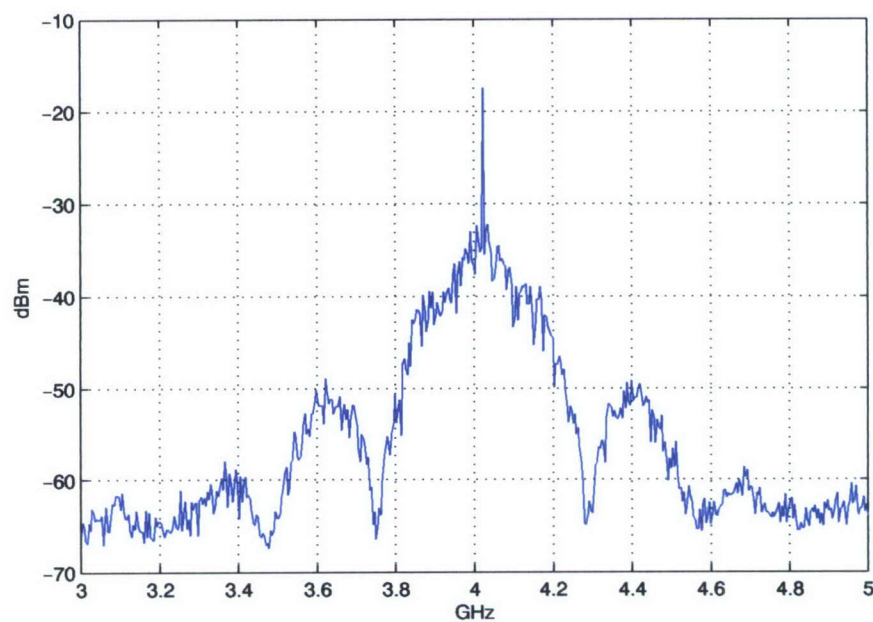


Figure 5.7: Spectrum of single-pulse waveform after modulation.

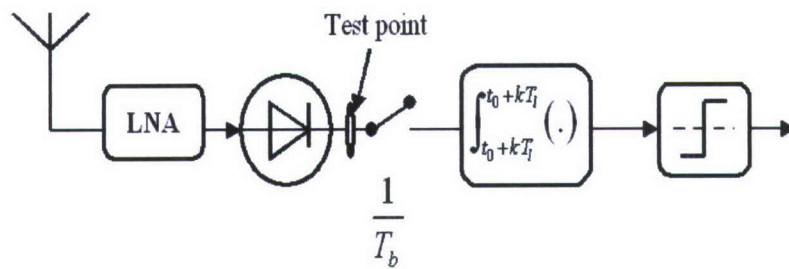


Figure 5.8: Receiver structure and test point.

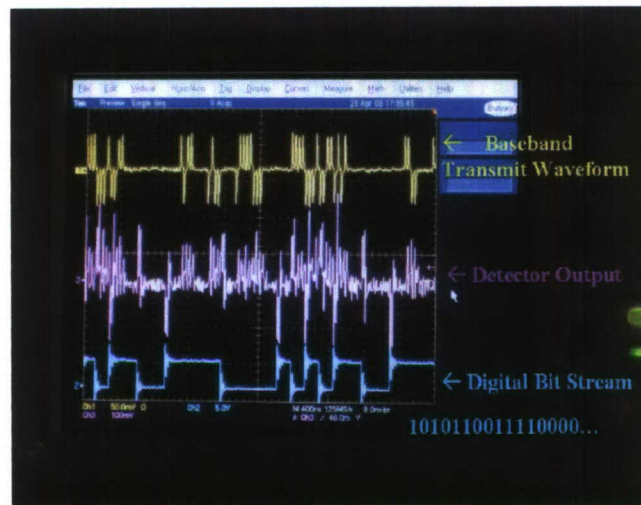


Figure 5.9: Time reversal waveform, system test result.



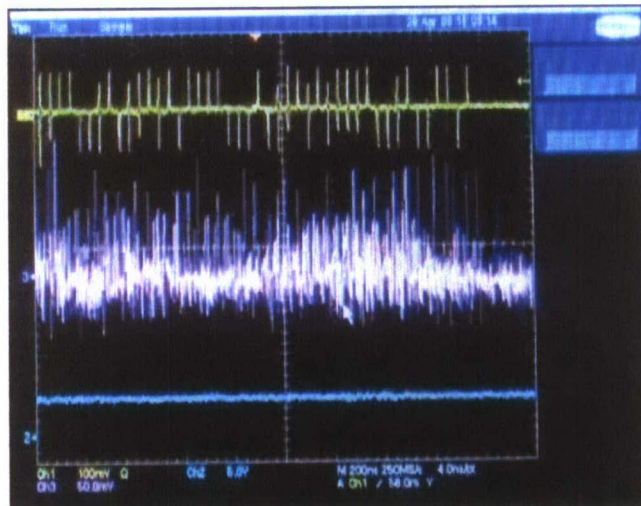


Figure 5.10: Single-pulse waveform, system test result.

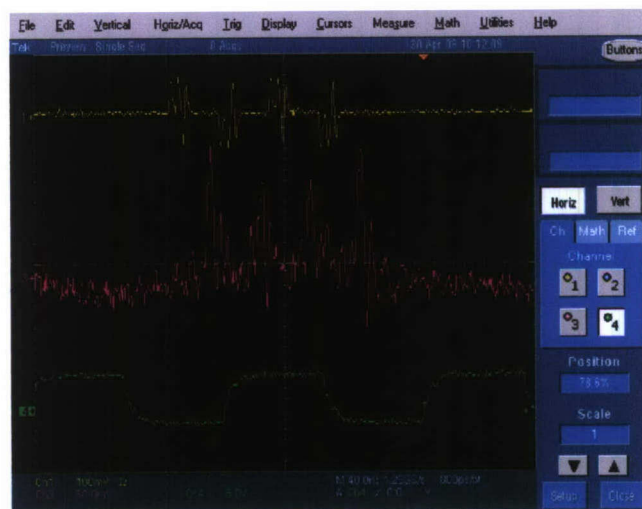


Figure 5.11: Time focusing property of time reversal.

## **Chapter 6**

# **Problems, Solutions and Lessons Gained**

### **6.1 Signal Integrity Issues**

Signal integrity engineering is about analysis and mitigation of various impairments on digital signal transmission at all levels of circuit connections. The causes include transmission delay, impedance matching, interference and cross talking, etc. The impairments become severe at high bit rates over longer distances. The signal integrity problem we face is mainly on the board-to-board connections between FPGA and mixed-signal devices (ADC and DAC). Since the clock rate is at 500 MHz, even the differential interface standards designed for high data rates cannot guarantee acceptable digital signal quality. The interface between the FPGA board and the DAC uses LVDS standard. We noticed that the unused DAC input ports can act as antennas to receive interference. We have grounded these input ports to eliminate the negative impact.

### **6.2 Carrier Leakage**

Although the modulator has very good carrier isolation (carrier feedthrough as low as -37 dBm), there are some other paths that the carrier can pass to the output port. Also, unbalanced bias between the two differential input ends leads to carrier contribution at the output. Conventional RF decoupling techniques can reduce carrier leakage. In addition, a narrow band notch filter at the carrier frequency may be employed to suppress the output carrier frequency.

### **6.3 Undesired Feedback via Parasitic Coupling**

One of difficulties for multi-stage RF circuits is to keep undesired feedback at a very low level. When frequency is high and bandwidth is large, the parasitic coupling becomes strong, which can easily push the amplifiers out of function due to RF feedback effect. We have noticed that at the receiver side there is some coupling between the digital output and the RF front-end, and self resonance can happen when the UWB receive antenna is close to the PCB. To make the circuit more stable, we need to improve RF shielding on the receiver RF board.

## 6.4 Some Lessons Gained

Tremendous effort has been made in developing the FPGA based digital back-ends. One lesson we have learned is that in the FPGA implementation phase time closure is very critical in dealing with nano-second-order signals, especially when the area usage is high (say, 80%). FPGA technology advances rapidly and many high-speed dense FPGA products are on the market. We have been using the latest Xilinx Virtex-5 FPGA chips in the test-bed, which truly lessens the in-chip timing problem. However, when we push the sampling rate higher and higher, the connection between the FPGA chips and the DAC or ADC becomes new bottle neck. In the transmitter side, this signal integrity problem prevents us from reaching higher clock rate beyond 500 MHz. In other words, to knock down this clock rate barrier we should seek a PCB-integrated FPGA/DAC solution.

## **Chapter 7**

### **Near Future Development Work**

The current version of our test-bed is able to program the transmit waveform for performance optimization, and we have used it to demonstrate time reversal phenomenon. However, this test-bed has some limitations on achieving the double distance goal. First, the link budget is not enough for a longer distance of interest and the dynamic range is too small. Second, the data rate is fixed in current version but scalability is highly demanded for a different propagation environments. Improvement effort will be on the receiver RF front-end and the digital back-ends at both sides. Specifically, major work items include redesigning frame structure, changing baseband structure, and adding low-noise amplifiers (maybe variable gain) to the receiver front-end. In addition, the following work should be considered too: improvement of synchronization scheme, adding AGC function, and making the threshold optimal or adaptive.







## **Part II**

## **Appendix**

## Chapter 8

# Automatic Instrumentation

### 8.1 Introduction

Various modern instruments and measuring devices in Wireless Networking Systems Lab (WNSL) have been used in the test-bed development and forward looking research. Finding efficient ways to operate these instruments and devices is a byproduct of our mainstream work. Controlling the instruments from a remote terminal allows us to make fast measurements. This in fact enables us to sound the channel and sense the environment more efficiently and precisely. Manually operation of instruments and measuring devices is not able to record measured data at fine intervals of time, such as at seconds or milliseconds level. Thus our tendency, to see how frequently the environment is changing, guided us to a new way of controlling the devices i.e. from a remote terminal. Our experimental setup consists of a Laptop/Computer having National Instrument's LabVIEW8.5 installed on it and USB-GPIB cable used for physical connection between instrument and Laptop/Computer. Here LabVIEW based computer serves as a remote terminal to control instrument automatically.

There are many other ways to control the instruments and measuring devices remotely. These include, control of instrument using Serial port or Ethernet etc.

### 8.2 LabVIEW Based Instrumentation

We started with the control of Agilent's N5230A PNA-L Vector network analyzer. Figure 8.1 shows the project layout.

Depending on the need we divided this project into two categories.

1 By recalling an already saved calibration file (.cst format) from the Instruments Hard disk.

- Project-Save Data Files.vi.
- Project-Capture Waveform.vi

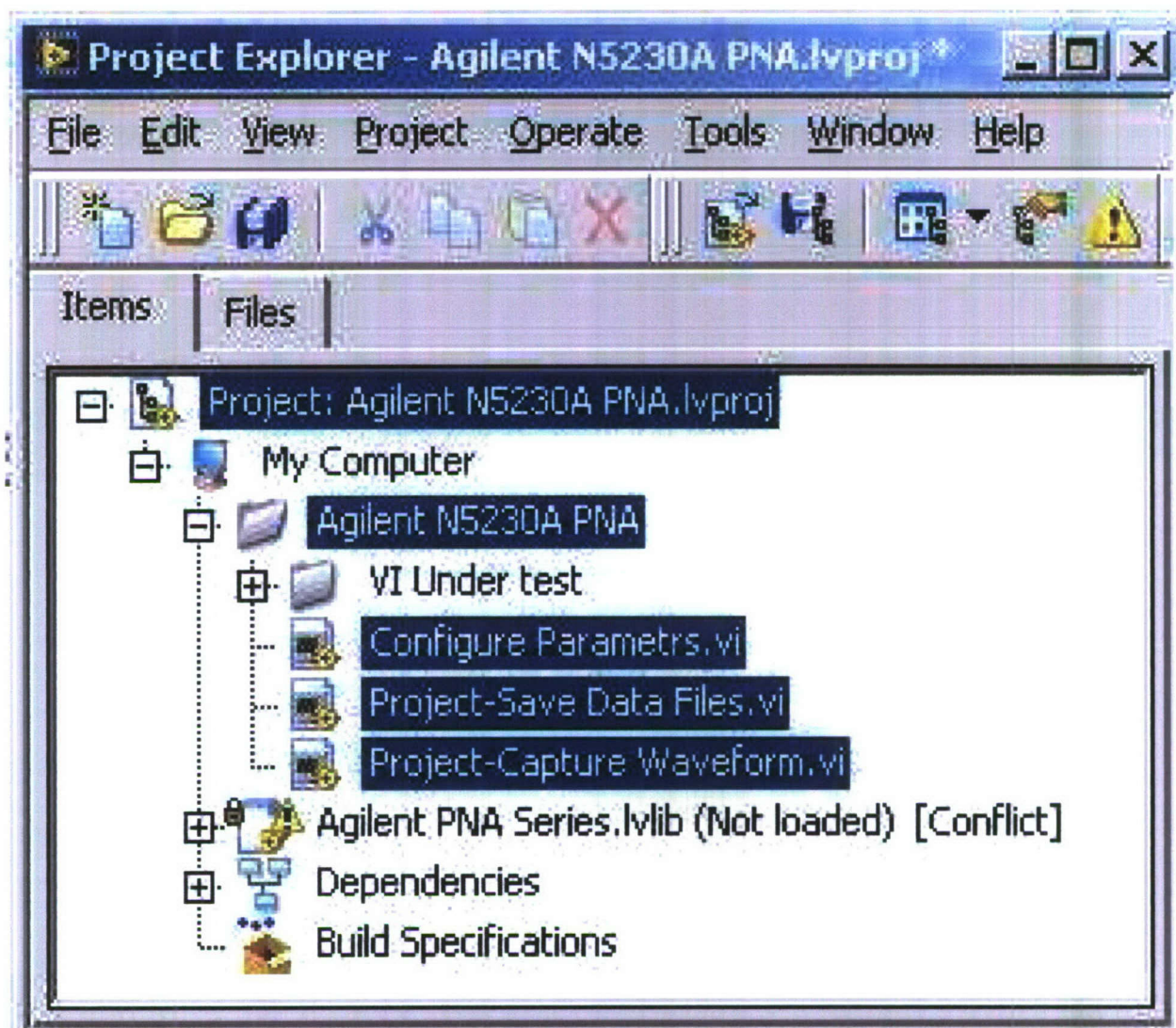


Figure 8.1: Project Layout



### 8.3. BY RECALLING AN ALREADY SAVED CALIBRATION FILE (.CST FORMAT) FROM THE INSTRUMENTS HARD

#### 2 Setting the network analyzer's parameters using LabVIEW.

- Configure Parameters.vi

Where, in the earlier case we are assuming that first we calibrate the instrument manually and save the calibration state at a particular location in PNA's hard disk. Then we use labVIEW to recall this saved calibration state and perform measurements. (A calibration state consists of all parameters like Start frequency, Stop frequency, Power level, Number of points, Sweep type, Sweep time etc.) While in the later case it is assumed that if we want to do the measurement with an uncorrected state i.e. non-calibrated state, then we can set the parameters like Start frequency, Stop frequency, Power level, Number of points, Sweep type, Sweep time etc from the remote terminal itself using LabVIEW8.5

### 8.3 By recalling an already saved calibration file (.cst format) from the Instruments Hard disk

#### A. Project-Save Data Files.vi

Following steps describe the working for saving the data files (CITI format) on the PNA's hard disk:

**Step 1:** Set all the required parameters shown in Table 8.1 and calibrate the instrument manually.

Table 8.1: PNA Settings

Parameter	Value
Start Frequency	3 GHz
Stop Frequency	4 GHz
Power Level	0 dBm
Average	Off
Number of points per sweep	1001
Sweep Type	Linear frequency
Trigger	Single

**Step 2:** Save the calibrated state in '.cst' format at a particular location on the network analyzer's hard disk.

**Step 3:** Open the LabVIEW program for saving data files.

**Step 4:** We can see the front Panel as shown in Figure 8.2.

**Step 5:** Now, the 'Select Instrument' column shows the GPIB address of all connected instruments (If more than one instrument are connected). So select one instrument showing 'GPIB0::16::INSTR', here 16 is the GPIB port number for our network analyzer.

**Step 6:** Now type the Path, File name and File format in following three boxes, of the saved calibration file. For example, in this case we stored a calibration file named '3g-4g-1001.cst' at 'D : \2008\0404\' path in network

Program to Save the Data files (.cti format) on VNA

Select Instrument	Type Path of Saved Cal. File	Type File Name of saved cal. file	Select Cal. File Format	Type Channel#
GPIB0::16::INSTR	D:\2008\0404\	3g-4g-1001	.cst 2	1
Type name of the .cti file to save		Select Measurement Type	Type Number of Traces to Record	Preset +1
MY_FILE		S21 2	100	Sweep +1
Date / Time				
<pre> 11:28:04.837\AM\;4/21/200811:28:04.788\AM\;4/21/200811:28:05.241\AM\;4/21/200811:28:05.679\AM\;4/21/200811:28:06.102\AM\;4/21/200811:28:06.524\AM\;4/21/200811:28:06.978\AM\;4/21/200811:28:07.416\AM\;4/21/200811:28:07.823\AM\;4/21/200811:28:08.245\AM\;4/21/200811:28:08.674\AM\;4/21/200811:28:09.103\AM\;4/21/200811:28:09.531\AM\;4/21/200811:28:09.959\AM\;4/21/200811:28:10.387\AM\;4/21/200811:28:10.815\AM\;4/21/200811:28:11.243\AM\;4/21/200811:28:11.671\AM\;4/21/200811:28:12.099\AM\;4/21/200811:28:12.527\AM\;4/21/200811:28:12.955\AM\;4/21/200811:28:13.383\AM\;4/21/200811:28:13.811\AM\;4/21/200811:28:14.239\AM\;4/21/200811:28:14.667\AM\;4/21/200811:28:15.095\AM\;4/21/200811:28:15.523\AM\;4/21/200811:28:15.951\AM\;4/21/200811:28:16.379\AM\;4/21/200811:28:16.807\AM\;4/21/200811:28:17.235\AM\;4/21/200811:28:17.663\AM\;4/21/200811:28:18.091\AM\;4/21/200811:28:18.519\AM\;4/21/200811:28:18.947\AM\;4/21/200811:28:19.375\AM\;4/21/200811:28:19.803\AM\;4/21/200811:28:20.231\AM\;4/21/200811:28:20.659\AM\;4/21/200811:28:21.087\AM\;4/21/200811:28:21.515\AM\;4/21/200811:28:21.943\AM\;4/21/200811:28:22.371\AM\;4/21/200811:28:22.799\AM\;4/21/200811:28:23.227\AM\;4/21/200811:28:23.655\AM\;4/21/200811:28:24.083\AM\;4/21/200811:28:24.511\AM\;4/21/200811:28:24.939\AM\;4/21/200811:28:25.367\AM\;4/21/200811:28:25.795\AM\;4/21/200811:28:26.223\AM\;4/21/200811:28:26.651\AM\;4/21/200811:28:27.079\AM\;4/21/200811:28:27.507\AM\;4/21/200811:28:27.935\AM\;4/21/200811:28:28.363\AM\;4/21/200811:28:28.791\AM\;4/21/200811:28:29.219\AM\;4/21/200811:28:29.647\AM\;4/21/200811:28:30.075\AM\;4/21/200811:28:30.503\AM\;4/21/200811:28:30.931\AM\;4/21/200811:28:31.359\AM\;4/21/200811:28:31.787\AM\;4/21/200811:28:32.215\AM\;4/21/200811:28:32.643\AM\;4/21/200811:28:33.071\AM\;4/21/200811:28:33.499\AM\;4/21/200811:28:33.927\AM\;4/21/200811:28:34.355\AM\;4/21/200811:28:34.783\AM\;4/21/200811:28:35.211\AM\;4/21/200811:28:35.639\AM\;4/21/200811:28:36.067\AM\;4/21/200811:28:36.495\AM\;4/21/200811:28:36.923\AM\;4/21/200811:28:37.351\AM\;4/21/200811:28:37.779\AM\;4/21/200811:28:38.207\AM\;4/21/200811:28:38.635\AM\;4/21/200811:28:39.063\AM\;4/21/200811:28:39.491\AM\;4/21/200811:28:39.919\AM\;4/21/200811:28:40.347\AM\;4/21/200811:28:40.775\AM\;4/21/200811:28:41.203\AM\;4/21/200811:28:41.631\AM\;4/21/200811:28:42.059\AM\;4/21/200811:28:42.487\AM\;4/21/200811:28:42.915\AM\;4/21/200811:28:43.343\AM\;4/21/200811:28:43.771\AM\;4/21/200811:28:44.199\AM\;4/21/200811:28:44.627\AM\;4/21/200811:28:45.055\AM\;4/21/200811:28:45.483\AM\;4/21/200811:28:45.911\AM\;4/21/200811:28:46.339\AM\;4/21/200811:28:46.767\AM\;4/21/200811:28:47.195\AM\;4/21/200811:28:47.623\AM\;4/21/200811:28:48.051\AM\;4/21/200811:28:48.479\AM\;4/21/200811:28:48.907\AM\;4/21/200811:28:49.335\AM\;4/21/200811:28:49.763\AM\;4/21/200811:28:50.191\AM\;4/21/200811:28:50.619\AM\;4/21/200811:28:51.047\AM\;4/21/200811:28:51.475\AM\;4/21/200811:28:51.903\AM\;4/21/200811:28:52.331\AM\;4/21/200811:28:52.759\AM\;4/21/200811:28:53.187\AM\;4/21/200811:28:53.615\AM\;4/21/200811:28:54.043\AM\;4/21/200811:28:54.471\AM\;4/21/200811:28:54.899\AM\;4/21/200811:28:55.327\AM\;4/21/200811:28:55.755\AM\;4/21/200811:28:56.183\AM\;4/21/200811:28:56.611\AM\;4/21/200811:28:57.039\AM\;4/21/200811:28:57.467\AM\;4/21/200811:28:57.895\AM\;4/21/200811:28:58.323\AM\;4/21/200811:28:58.751\AM\;4/21/200811:28:59.179\AM\;4/21/200811:28:59.607\AM\;4/21/200811:29:00.035\AM\;4/21/200811:29:00.463\AM\;4/21/200811:29:00.891\AM\;4/21/200811:29:01.319\AM\;4/21/200811:29:01.747\AM\;4/21/200811:29:02.175\AM\;4/21/200811:29:02.603\AM\;4/21/200811:29:03.031\AM\;4/21/200811:29:03.459\AM\;4/21/200811:29:03.887\AM\;4/21/200811:29:04.315\AM\;4/21/200811:29:04.743\AM\;4/21/200811:29:05.171\AM\;4/21/200811:29:05.599\AM\;4/21/200811:29:06.027\AM\;4/21/200811:29:06.455\AM\;4/21/200811:29:06.883\AM\;4/21/200811:29:07.311\AM\;4/21/200811:29:07.739\AM\;4/21/200811:29:08.167\AM\;4/21/200811:29:08.595\AM\;4/21/200811:29:09.023\AM\;4/21/200811:29:09.451\AM\;4/21/200811:29:09.879\AM\;4/21/200811:29:10.307\AM\;4/21/200811:29:10.735\AM\;4/21/200811:29:11.163\AM\;4/21/200811:29:11.591\AM\;4/21/200811:29:12.019\AM\;4/21/200811:29:12.447\AM\;4/21/200811:29:12.875\AM\;4/21/200811:29:13.303\AM\;4/21/200811:29:13.731\AM\;4/21/200811:29:14.159\AM\;4/21/200811:29:14.587\AM\;4/21/200811:29:15.015\AM\;4/21/200811:29:15.443\AM\;4/21/200811:29:15.871\AM\;4/21/200811:29:16.299\AM\;4/21/200811:29:16.727\AM\;4/21/200811:29:17.155\AM\;4/21/200811:29:17.583\AM\;4/21/200811:29:18.011\AM\;4/21/200811:29:18.439\AM\;4/21/200811:29:18.867\AM\;4/21/200811:29:19.295\AM\;4/21/200811:29:19.723\AM\;4/21/200811:29:20.151\AM\;4/21/200811:29:20.579\AM\;4/21/200811:29:21.007\AM\;4/21/200811:29:21.435\AM\;4/21/200811:29:21.863\AM\;4/21/200811:29:22.291\AM\;4/21/200811:29:22.719\AM\;4/21/200811:29:23.147\AM\;4/21/200811:29:23.575\AM\;4/21/200811:29:24.003\AM\;4/21/200811:29:24.431\AM\;4/21/200811:29:24.859\AM\;4/21/200811:29:25.287\AM\;4/21/200811:29:25.715\AM\;4/21/200811:29:26.143\AM\;4/21/200811:29:26.571\AM\;4/21/200811:29:26.999\AM\;4/21/200811:29:27.427\AM\;4/21/200811:29:27.855\AM\;4/21/200811:29:28.283\AM\;4/21/200811:29:28.711\AM\;4/21/200811:29:29.139\AM\;4/21/200811:29:29.567\AM\;4/21/200811:29:30.005\AM\;4/21/200811:29:30.433\AM\;4/21/200811:29:30.861\AM\;4/21/200811:29:31.289\AM\;4/21/200811:29:31.717\AM\;4/21/200811:29:32.145\AM\;4/21/200811:29:32.573\AM\;4/21/200811:29:33.001\AM\;4/21/200811:29:33.429\AM\;4/21/200811:29:33.857\AM\;4/21/200811:29:34.285\AM\;4/21/200811:29:34.713\AM\;4/21/200811:29:35.141\AM\;4/21/200811:29:35.569\AM\;4/21/200811:29:35.997\AM\;4/21/200811:29:36.425\AM\;4/21/200811:29:36.853\AM\;4/21/200811:29:37.281\AM\;4/21/200811:29:37.709\AM\;4/21/200811:29:38.137\AM\;4/21/200811:29:38.565\AM\;4/21/200811:29:38.993\AM\;4/21/200811:29:39.421\AM\;4/21/200811:29:39.849\AM\;4/21/200811:29:40.277\AM\;4/21/200811:29:40.705\AM\;4/21/200811:29:41.133\AM\;4/21/200811:29:41.561\AM\;4/21/200811:29:41.989\AM\;4/21/200811:29:42.417\AM\;4/21/200811:29:42.845\AM\;4/21/200811:29:43.273\AM\;4/21/200811:29:43.701\AM\;4/21/200811:29:44.129\AM\;4/21/200811:29:44.557\AM\;4/21/200811:29:44.985\AM\;4/21/200811:29:45.413\AM\;4/21/200811:29:45.841\AM\;4/21/200811:29:46.269\AM\;4/21/200811:29:46.697\AM\;4/21/200811:29:47.125\AM\;4/21/200811:29:47.553\AM\;4/21/200811:29:47.981\AM\;4/21/200811:29:48.409\AM\;4/21/200811:29:48.837\AM\;4/21/200811:29:49.265\AM\;4/21/200811:29:49.693\AM\;4/21/200811:29:50.121\AM\;4/21/200811:29:50.549\AM\;4/21/200811:29:50.977\AM\;4/21/200811:29:51.405\AM\;4/21/200811:29:51.833\AM\;4/21/200811:29:52.261\AM\;4/21/200811:29:52.689\AM\;4/21/200811:29:53.117\AM\;4/21/200811:29:53.545\AM\;4/21/200811:29:53.973\AM\;4/21/200811:29:54.401\AM\;4/21/200811:29:54.829\AM\;4/21/200811:29:55.257\AM\;4/21/200811:29:55.685\AM\;4/21/200811:29:56.113\AM\;4/21/200811:29:56.541\AM\;4/21/200811:29:56.969\AM\;4/21/200811:29:57.397\AM\;4/21/200811:29:57.825\AM\;4/21/200811:29:58.253\AM\;4/21/200811:29:58.681\AM\;4/21/200811:29:59.109\AM\;4/21/200811:29:59.537\AM\;4/21/200811:29:59.965\AM\;4/21/200811:30:00.393\AM\;4/21/200811:30:00.821\AM\;4/21/200811:30:01.249\AM\;4/21/200811:30:01.677\AM\;4/21/200811:30:02.105\AM\;4/21/200811:30:02.533\AM\;4/21/200811:30:02.961\AM\;4/21/200811:30:03.389\AM\;4/21/200811:30:03.817\AM\;4/21/200811:30:04.245\AM\;4/21/200811:30:04.673\AM\;4/21/200811:30:05.101\AM\;4/21/200811:30:05.529\AM\;4/21/200811:30:05.957\AM\;4/21/200811:30:06.385\AM\;4/21/200811:30:06.813\AM\;4/21/200811:30:07.241\AM\;4/21/200811:30:07.669\AM\;4/21/200811:30:08.097\AM\;4/21/200811:30:08.525\AM\;4/21/200811:30:08.953\AM\;4/21/200811:30:09.381\AM\;4/21/200811:30:09.809\AM\;4/21/200811:30:10.237\AM\;4/21/200811:30:10.665\AM\;4/21/200811:30:11.093\AM\;4/21/200811:30:11.521\AM\;4/21/200811:30:11.949\AM\;4/21/200811:30:12.377\AM\;4/21/200811:30:12.805\AM\;4/21/200811:30:13.233\AM\;4/21/200811:30:13.661\AM\;4/21/200811:30:14.089\AM\;4/21/200811:30:14.517\AM\;4/21/200811:30:14.945\AM\;4/21/200811:30:15.373\AM\;4/21/200811:30:15.801\AM\;4/21/200811:30:16.229\AM\;4/21/200811:30:16.657\AM\;4/21/200811:30:17.085\AM\;4/21/200811:30:17.513\AM\;4/21/200811:30:17.941\AM\;4/21/200811:30:18.369\AM\;4/21/200811:30:18.797\AM\;4/21/200811:30:19.225\AM\;4/21/200811:30:19.653\AM\;4/21/200811:30:20.081\AM\;4/21/200811:30:20.509\AM\;4/21/200811:30:20.937\AM\;4/21/200811:30:21.365\AM\;4/21/200811:30:21.793\AM\;4/21/200811:30:22.221\AM\;4/21/200811:30:22.649\AM\;4/21/200811:30:23.077\AM\;4/21/200811:30:23.505\AM\;4/21/200811:30:23.933\AM\;4/21/200811:30:24.361\AM\;4/21/200811:30:24.789\AM\;4/21/200811:30:25.217\AM\;4/21/200811:30:25.645\AM\;4/21/200811:30:26.073\AM\;4/21/200811:30:26.501\AM\;4/21/200811:30:26.929\AM\;4/21/200811:30:27.357\AM\;4/21/200811:30:27.785\AM\;4/21/200811:30:28.213\AM\;4/21/200811:30:28.641\AM\;4/21/200811:30:29.069\AM\;4/21/200811:30:29.497\AM\;4/21/200811:30:29.925\AM\;4/21/200811:30:30.353\AM\;4/21/200811:30:30.781\AM\;4/21/200811:30:31.209\AM\;4/21/200811:30:31.637\AM\;4/21/200811:30:32.065\AM\;4/21/200811:30:32.493\AM\;4/21/200811:30:32.921\AM\;4/21/200811:30:33.349\AM\;4/21/200811:30:33.777\AM\;4/21/200811:30:34.205\AM\;4/21/200811:30:34.633\AM\;4/21/200811:30:35.061\AM\;4/21/200811:30:35.489\AM\;4/21/200811:30:35.917\AM\;4/21/200811:30:36.345\AM\;4/21/200811:30:36.773\AM\;4/21/200811:30:37.201\AM\;4/21/200811:30:37.629\AM\;4/21/200811:30:38.057\AM\;4/21/200811:30:38.485\AM\;4/21/200811:30:38.913\AM\;4/21/200811:30:39.341\AM\;4/21/200811:30:39.769\AM\;4/21/200811:30:40.197\AM\;4/21/200811:30:40.625\AM\;4/21/200811:30:41.053\AM\;4/21/200811:30:41.481\AM\;4/21/200811:30:41.909\AM\;4/21/200811:30:42.337\AM\;4/21/200811:30:42.765\AM\;4/21/200811:30:43.193\AM\;4/21/200811:30:43.621\AM\;4/21/200811:30:44.049\AM\;4/21/200811:30:44.477\AM\;4/21/200811:30:44.905\AM\;4/21/200811:30:45.333\AM\;4/21/200811:30:45.761\AM\;4/21/200811:30:46.189\AM\;4/21/200811:30:46.617\AM\;4/21/200811:30:47.045\AM\;4/21/200811:30:47.473\AM\;4/21/200811:30:47.901\AM\;4/21/200811:30:48.329\AM\;4/21/200811:30:48.757\AM\;4/21/200811:30:49.185\AM\;4/21/200811:30:49.613\AM\;4/21/200811:30:50.041\AM\;4/21/200811:30:50.469\AM\;4/21/200811:30:50.897\AM\;4/21/200811:30:51.325\AM\;4/21/200811:30:51.753\AM\;4/21/200811:30:52.181\AM\;4/21/200811:30:52.609\AM\;4/21/200811:30:53.037\AM\;4/21/200811:30:53.465\AM\;4/21/200811:30:53.893\AM\;4/21/200811:30:54.321\AM\;4/21/200811:30:54.749\AM\;4/21/200811:30:55.177\AM\;4/21/200811:30:55.605\AM\;4/21/200811:30:56.033\AM\;4/21/200811:30:56.461\AM\;4/21/200811:30:56.889\AM\;4/21/200811:30:57.317\AM\;4/21/200811:30:57.745\AM\;4/21/200811:30:58.173\AM\;4/21/200811:30:58.601\AM\;4/21/200811:30:59.029\AM\;4/21/200811:30:59.457\AM\;4/21/200811:30:59.885\AM\;4/21/200811:31:00.313\AM\;4/21/200811:31:00.741\AM\;4/21/200811:31:01.169\AM\;4/21/200811:31:01.597\AM\;4/21/200811:31:02.025\AM\;4/21/200811:31:02.453\AM\;4/21/200811:31:02.881\AM\;4/21/200811:31:03.309\AM\;4/21/200811:31:03.737\AM\;4/21/200811:31:04.165\AM\;4/21/200811:31:04.593\AM\;4/21/200811:31:05.021\AM\;4/21/200811:31:05.449\AM\;4/21/200811:31:05.877\AM\;4/21/200811:31:06.305\AM\;4/21/200811:31:06.733\AM\;4/21/200811:31:07.161\AM\;4/21/200811:31:07.589\AM\;4/21/200811:31:08.017\AM\;4/21/200811:31:08.445\AM\;4/21/200811:31:08.873\AM\;4/21/200811:31:09.301\AM\;4/21/200811:31:09.729\AM\;4/21/200811:31:10.157\AM\;4/21/200811:31:10.585\AM\;4/21/200811:31:11.013\AM\;4/21/200811:31:11.441\AM\;4/21/200811:31:11.869\AM\;4/21/200811:31:12.297\AM\;4/21/200811:31:12.725\AM\;4/21/200811:31:13.153\AM\;4/21/200811:31:13.581\AM\;4/21/200811:31:14.009\AM\;4/21/200811:31:14.437\AM\;4/21/200811:31:14.865\AM\;4/21/200811:31:15.293\AM\;4/21/200811:31:15.721\AM\;4/21/200811:31:16.149\AM\;4/21/200811:31:16.577\AM\;4/21/200811:31:17.005\AM\;4/21/200811:31:17.433\AM\;4/21/200811:31:17.861\AM\;4/21/200811:31:18.289\AM\;4/21/200811:31:18.717\AM\;4/21/200811:31:19.145\AM\;4/21/200811:31:19.573\AM\;4/21/200811:31:20.001\AM\;4/21/200811:31:20.429\AM\;4/21/200811:31:20.857\AM\;4/21/200811:31:21.285\AM\;4/21/200811:31:21.713\AM\;4/21/200811:31:22.141\AM\;4/21/200811:31:22.569\AM\;4/21/200811:31:22.997\AM\;4/21/200811:31:23.425\AM\;4/21/200811:31:23.853\AM\;4/21/200811:31:24.281\AM\;4/21/200811:31:24.709\AM\;4/21/200811:31:25.137\AM\;4/21/200811:31:25.565\AM\;4/21/200811:31:25.993\AM\;4/21/200811:31:26.421\AM\;4/21/200811:31:26.849\AM\;4/21/200811:31:27.277\AM\;4/21/200811:31:27.705\AM\;4/21/200811:31:28.133\AM\;4/21/200811:31:28.561\AM\;4/21/200811:31:28.989\AM\;4/21/200811:31:29.417\AM\;4/21/20</pre>				



analyzer. So we typed 'D : \2008\0404\' in the File path, '3g-4g-1001' in the file name and selected '.cst' file format from the menu respectively as shown in Figure 8.2. In the File format type column we have three options to select, i.e. 0 means '.sta', 1 means '.cal' and 2 means '.cst', this option number is shown in the next little box.

**Step 7:** Now type the file name 'MY\_FILE in this case' in the next column named 'Type name of the .cti file to save'. As we are attempting to save many data files automatically. So it is needed that the program will automatically generate the file names. Thus we modified the program in such a manner that it will start appending numeric numbers (in ascending order) to the given filename. Thus reducing time to save each file and avoiding the duplicate file name problem.

**Step 8:** Here we specify the measurement type, i.e. S11, S12, S21, S22 and the next box shows option numbers for measurement type. Where, 0 means 'S11', 1 means 'S12', 2 means 'S21' and 3 means 'S22'. As shown in Figure 8.2.

**Step 9:** In the space provided under 'Type number of traces to Record' fill in as many data files as needed. After execution, program stops automatically when this number is achieved. We performed for saving data-files for upto 500 traces in our lab. But as shown in Figure 8.2 this number is 100.

**Step 10:** The string block named 'Date / Time' shows current date and time taken to save each CITI data file. Here blank space is represented by '/s' word.

After completion of program we can use flash drive to copy saved data from network analyzer to other PC, where we do further Matlab processing.

Two flags, 'Preset' and 'Sweep' are included to check the program flow. Flag value '+1' means program is running ok and '0' means there is an error before the flag value is achieved. Also, if there is an error then error number and its description are shown in error out box.

### **B. Project-Capture Waveform.vi**

The other functionality is to capture the waveform from network analyzer. Figure 8.3 shows the labVIEW front panel of captured waveform. This program also follows exactly same Steps[1,2,5,6,7,8,9,10] as discussed above. But here our purpose is to observe the waveforms as shown on network analyzer's screen. So instead of generating any filename, we put a graphic display, which enables us to see the captured waveform. The X- axis is frequency in Hz and Y- Axis is magnitude power in dbm. The X- and Y- axis scales are set to auto adjusting mode, for example in this case, we set Start frequency = 3GHz and Stop frequency = 4GHz, so we can see the X-axis scale shows frequency range starting from 3GHz to 4 GHz. We can also copy the captured trace from LabVIEW front panel and then can save as JPG file etc.

## **8.4 Setting the network analyzers parameters using LabVIEW**

### **A. Configure Parameters.vi**

Apart from the procedure mentioned in then above section, we have an additional program to configure various parameters such as Channel number, Power, Average, Start / Stop frequency, Number of points and Sweep type etc. Figure 8.4 shows LabVIEW front panel for 'configure parameters.vi' program. But we rarely need this program, as

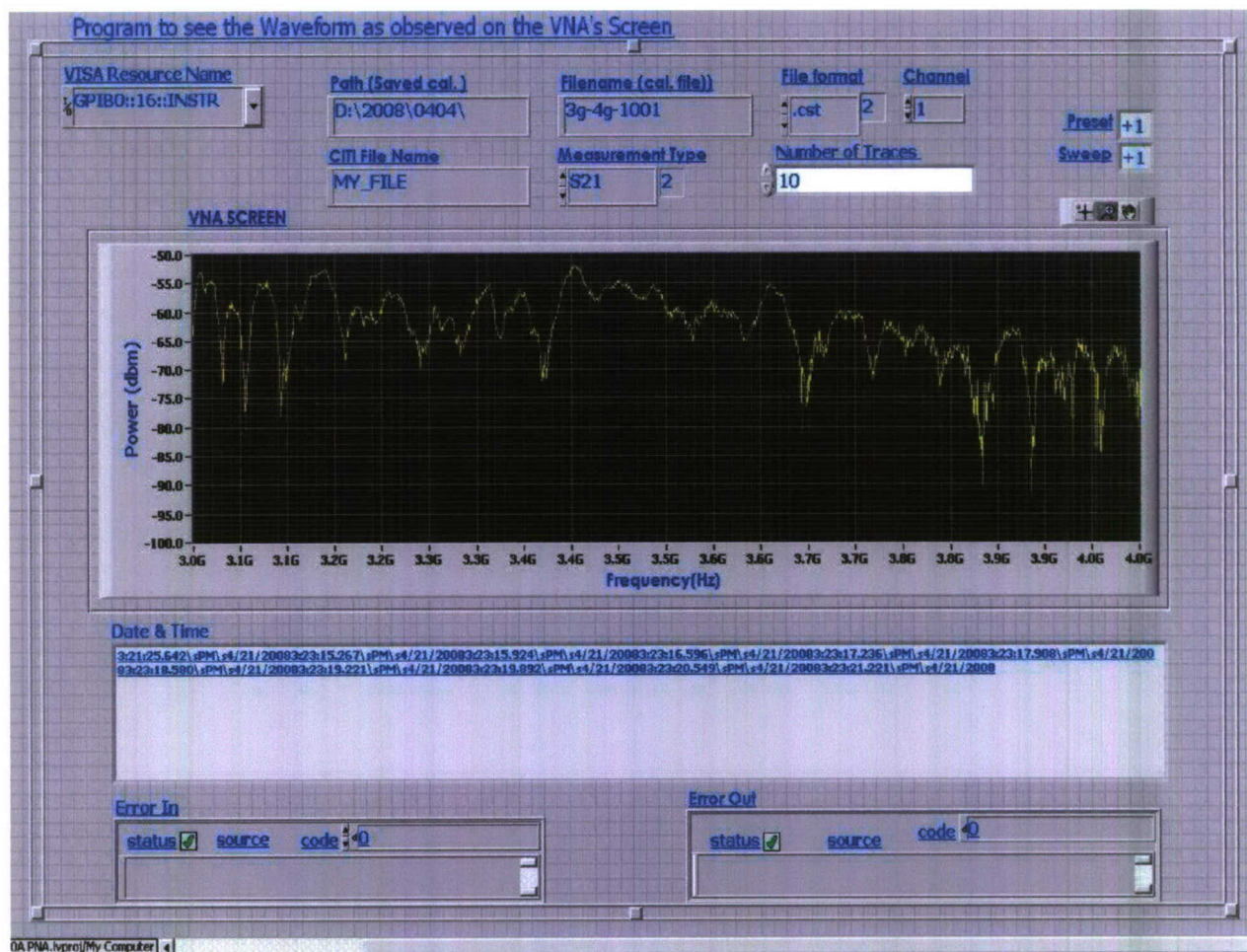


Figure 8.3: Project Capture Waveform



this can be used only when we want to do the measurement with an uncorrected state i.e. non-calibrated state. So in that case we can set the basic parameters for measurement from the remote terminal itself using LabVIEW8.5

CONFIGURE THE CH, POWER, AVERAGE, START/STOP FREQUENCY AND NUMBER OF POINTS FOR AGILENT N5230A PNA

Resource Name In: GPIB::16::INSTR

Channel: 1

Power Level (dbm): 0.00

Average: On

Average Count: 1

Start freq: 3.00G

Stop freq: 5.00G

Auto Sweep: On

Sweep Points: 1001

Sweep Type: Linear Frequency

Sweep Gen Type: Analog

Sweep / Dwell Time: 6.03

Error In (no error): status code: 0, source:

Resource Out- Average: GPIB::16::INSTR

Error Out - Average: status code: 0, source:

Resource Out- Frequency: GPIB::16::INSTR

Error Out- Frequency: status code: 0, source:

Resource Out- Power: GPIB::16::INSTR

Error Out- Power: status code: 0, source:

Resource Out- Sweep Points: GPIB::16::INSTR

Error Out- Sweep Points: status code: 0, source:

Figure 8.4: Configure Parameters

The working of this program is very simple, All we need to know is the Channel Number to use, Power Level, Average, Average count, Start frequency, Stop frequency, Sweep settings and number of points per sweep. After typing each values in respective fields, select 'GPIB::16::INSTR' in the 'Resource Name In' column and run the program once. We can observe the new settings on the network analyzer's screen.

We have some more instruments in our wireless networking systems lab.

These are:

- Spectrum Analyzer (FSEM-20) manufactured by Rohde & Schwarz.

- Communication signal analyzer (CSA-8000) manufactured by Tektronix.

Our emphasis is to command all of these instruments using labVIEW so that we will be able to record real time data as fast as possible.

## Chapter 9

# Local Oscillator: A Key Device Toward Wideband Cognitive Radio

### 9.1 Introduction

One potential evolution for our current test-bed is to be a wideband cognitive radio system. To achieve this goal, we need to add a spectrum scanning module and change the RF part, while the baseband processing can be handled by our current FPGA platform.

The novel characteristic of cognitive radio transceiver is a wideband sensing capability of the RF front-end. This function is mainly related to RF hardware technologies such as wideband antenna, power amplifier, automatic gain controller (AGC) and local oscillator(LO). RF hardware for the cognitive radio should be capable of tuning to any part of a large range of frequency spectrum. Also such spectrum sensing enables real-time measurements of spectrum information from radio environment. Figure 9.1 shows a typical architecture of wideband RF/analog front-end.

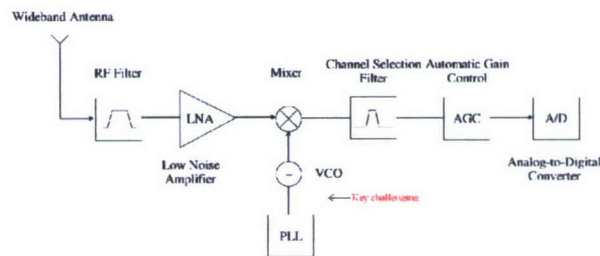


Figure 9.1: The architecture of cognitive radio wideband RF analog front-end.

In wideband systems such as the UWB cognitive radio system, proper LO signal generation is the most challenging issue in RF front-end because it must cover a wide frequency range and consume very little power in doing it, as well as switch its frequency at a very fast speed.



In order to address this RF agility challenge and get ready to develop our next generation test-bed, A survey on this kind of frequency synthesizer and voltage-controlled oscillator (VCO) was carried out.

## 9.2 VCO and PLL

A LO mainly consists of a VCO and a precise Phase locked loop (PLL). Figure 9.2 shows the architecture of a standard PLL based frequency synthesizer.

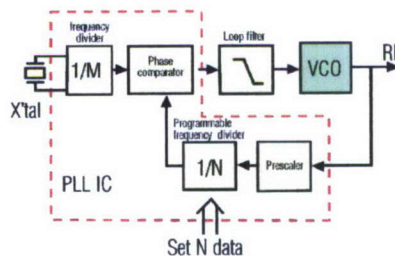


Figure 9.2: The diagram of PLL based frequency synthesizer.

**VCO:** The VCO generates a signal at a specific frequency for a given voltage to mix with the incoming signal. This procedure converts the incoming signal to baseband or an intermediate frequency.

Wideband VCOs are used in a variety of RF and microwave systems, including broadband measurement equipment, wireless and TV applications and military electronic countermeasures (ECM) systems. In modern ECM systems, they serve as the frequency-agile local oscillators in receiver subsystems and fast-modulation noise sources in active jamming subsystems. Among wideband tunable signal sources such as YIG-tuned oscillators, wideband VCOs are preferable because of their small size, low weight, high settling time speed and capability of fully monolithic integration. Therefore, modern radar and communication applications demand VCOs that are capable of being swept across a wide range of potential threat frequencies with a speed and settling time far beyond those of the YIG-tuned oscillators.

In spectrum sensing, frequency-hopping synthesizer requires very fast frequency switching time. One can build several VCOs and dividers to generate all the required tones; however, it may dissipate a lot of power. Another approach is to utilize single-sideband mixers. This approach may produce all the frequency tones by using one or two synthesizers. However, the traditional single-sideband mixers dissipate much power and usually suffer from spurious spectrum purity.

**PLL:** The PLL ensures that a signal is locked on a specific frequency and can also be used to generate precise frequencies with fine resolution. A PLL is a control system that generates a signal that has a fixed relation to the phase of a "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. A phase-locked loop is an example of a control system using negative feedback.

PLL are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital



logic designs such as microprocessors. Since a single integrated circuit can provide a complete PLL building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a cycle per second up to many gigahertz.

### 9.3 Products Available on Market

For frequency synthesizer, the product available on market can support a large frequency range with a very fast switching speed. But most of such wideband frequency synthesizers are in big size, which are not proper for cognitive radio use, otherwise, some products have small size, but don't support fast switching speed.

With respect to switching speed, the Model 10512 VCO from Narda Microwave-East, INC. is the fastest one. Model 10512 employs two VCOs, While the tuning time for a single VCO is less than 100 ns, switching time between two retuned VCOs via the high-speed switch is less than 15 ns.

- Model 10512 VCO by Narda Microwave-East, INC.



Figure 9.3: Model 10512 by Narda Microwave-East, INC.

The standard Model 10512 has a frequency range of 2.8 to 3.2 GHz, but other frequencies can be accommodated well into the millimeter-wave region. It consumes only 11 W, measures 4 in. x 4 in. x 0.6 in, weighs less than 1 oz,

With respect to wide output frequency range of frequency synthesizers or VCOs, the following is a glance of available products.

- Frequency synthesizer FSFS315555-500 by Synergy Microwave Corp.

The FSFS315555-500 features:

Frequency Range: 3150 to 5550 MHz.

Step Size: 5 MHz.

Settling Time: less than 50  $\mu$ s.

Output Power: +5 dBm.

Phase Noise: -100 dBc/Hz (Typ.) offset @ 1 MHz Package Size: SMT package 1.0in x 1.25in.

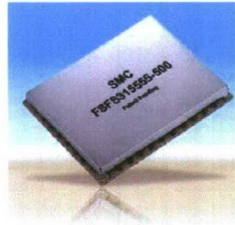


Figure 9.4: FSFS315555-500 by Synergy Microwave Corp.

- Frequency Synthesizers by Receiver Systems Division of Wide Band Systems, INC.

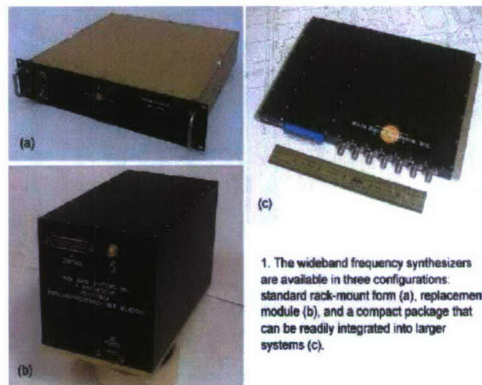


Figure 9.5: Frequency synthesizers by Wide Band Systems, INC.

Features:

Frequency Range: 2.0 to 18.0 GHz.

Switching Speed: 5  $\mu$ s maximum (3  $\mu$ s typical).

Frequency Resolution: as slow as 5.0 KHz.

Step Size: (12.7mm x 195mm x 135 mm).

Power Consumption: only 22W DC.

The output of this product can be a sequence of frequencies, a sequence of RF pulses, a sequence of amplitudes, or any combination of frequency, timing, and amplitude sequences desired.

- Model 2126 Fast Switching Synthesizer by Aeroflex, Inc.

Features:

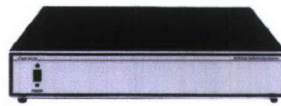


Figure 9.6: Model 2126 fast switching synthesizer by Aeroflex, Inc.

Frequency Range: 4.5 to 6010 MHz.

Switching Speed: Less than 100 microsecond switching

Frequency Resolution: 1 Hz.

Low spurious.

- UFS 0.3-40 GHz Ultra Wide Band Frequency Synthesizer by Elcom, INC.



Figure 9.7: UFS 0.3-40 GHz Ultra Wideband frequency synthesizer.

Features:

Frequency Range:

UFS-3: 0.3 to 3 GHz.

UFS-18: 0.3 to 18 GHz.

Custom: 0.01 to 54 GHz.

Ultra-Fast Switching Speed: 250 ns, Full Band.

Frequency Resolution: 1 Hz resolution.

Low Phase Noise Floor: -150 dBc up to 20 GHz.

Low Phase Noise: -135 dBc 1 MHz offset @ 10 GHz.

Exceptionally Clean Signal: -68 dBc Spurious, -50 dBc Harmonics.

- AtlanTecRF Frequency Synthesizer.

It features 5 to 14.55 GHz frequency range, 500 kHz resolution, and measures 33mm x 88mm x 16 mm.

- STMicroelectronics STW8110x Frequency Synthesizer.

The STMicroelectronics STW8110x is an integrated RF synthesizer with two voltage controlled oscillators (VCOs). Showing high performance, high integration, low power, and multi-band performances:

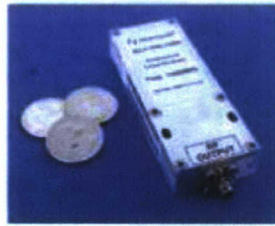


Figure 9.8: AtlanTecRF frequency synthesizer.

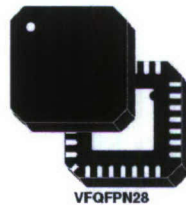


Figure 9.9: STMicroelectronics STW8110x frequency synthesizer.

STW81102: 3000 - 3620 MHz and 4000 - 4650 MHz (direct output).

STW81103: 2500 - 3050 MHz and 4350 - 5000 MHz (direct output).

Excellent integrated phase noise.

Fast lock time is 150  $\mu$ s.

Small size exposed pad VFQFPN28 package with 5mm x 5mm x 1.0mm dimension.

- PLL evaluation kit by Synergy Microwave Corp.

#### Features:

Frequency Range: 2000 - 4000 MHz.

Step Size: 1000 kHz.

Settling Time: less than 8 ms.

Typical Phase Noise: -110 dbc/Hz @100 kHz

- Surface Mount Frequency Synthesizer by General Electronic Devices, INC.

#### Features:

Frequency Range: 3500 MHz to 4500 MHz.

Frequency Resolution: 1 MHz.

Output Power: +7 dBm 2.5 dB.

Harmonic: -30 dBc Typ.



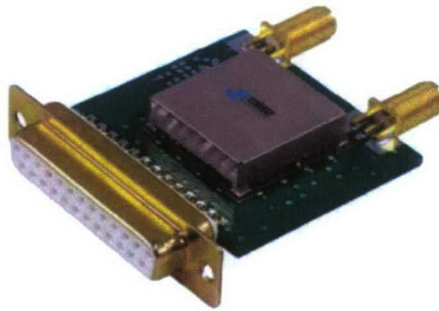


Figure 9.10: PLL evaluation kit by Synergy Microwave Corp.



Figure 9.11: Model LMPL B 4000 frequency synthesizer by General Electronic Devices, INC.

Spurious: -65 dBc Typ.

Phase Noise @ 1500MHz Output(Internal Ref.): -75dBc/Hz @ 10 KHz Offset, and -95dBc/Hz @ 100 KHz Offset.

- Si4133 RF Synthesizer by Silicon Laboratories, Inc.

This Dual-band RF Synthesizers features:

RF1: 900 MHz to 1.8 GHz.

RF2: 750 MHz to 1.5 GHz.

IF Synthesizer: IF 62.5 MHz to 1.0 GHz.

Fast settling time: 200  $\mu$ s for GSM/DCS1800 applications.

Fully integrated VCO and programmable loop filters and Small-outline, 24-pin package (TSSOP).



Figure 9.12: Si4133 RF synthesizer by Silicon Laboratories, Inc.

- SMT Wideband MMIC VCOs by Hittite Microwave Corporation.



Frequency (GHz)	Tuning Voltage (V)	Output Power (dBm)	10 kHz SSB Phase Noise (dBc/Hz)	100 kHz SSB Phase Noise (dBc/Hz)	Tuning Port Bandwidth (MHz)	Bias Supply	Part Number
4 - 8	0 to +20	+6	-76	-106	30	+5V@56mA	HMC586LC4B
5 - 10	0 to +20	+6	-73	-98	30	+5V@58mA	HMC587LC4B
8 - 12.5	0 to +15	+5	-63	-93	65	+5V@56mA	HMC588LC4B

Figure 9.13: SMT Wideband MMIC VCOs by Hittite Microwave Corporation.

- Wide Band VCO by Silvers IMA Sweden.



Figure 9.14: Wideband VCO by Silvers IMA Sweden, INC.

This VCO features:

Frequency Range: 3.0- 5.0 GHz.

Tuning Voltage: 0 +20 V.

Output Power: Overall 14 to 19 dBm.

Slew Rate: 20 GHz/ $\mu$ s.

Dimensions: 20.7mm x 14.1mm x 2.5mm.

- Voltage Tuned Oscillator by Phase Matrix Inc.

This VTO features:

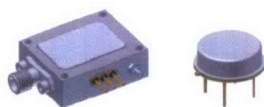


Figure 9.15: Voltage tuned oscillator by Phase Matrix, Inc.

Operating Frequencies: 4 to 8 GHz.

Output Power: 10 dBm Typ.

Tuning Sensitivity Ratio: 2:1 max.

Tuning Voltage: 0 to 20 Volts.

Low Phase Noise: less than -95 dBc/Hz @100 KHz.